

Compal Confidential

Model Name : VIUS3/S4  
File Name : LA-8951PR01  
BOM P/N:43

# Compal Confidential

## VIUS3/S4 M/B Schematics Document

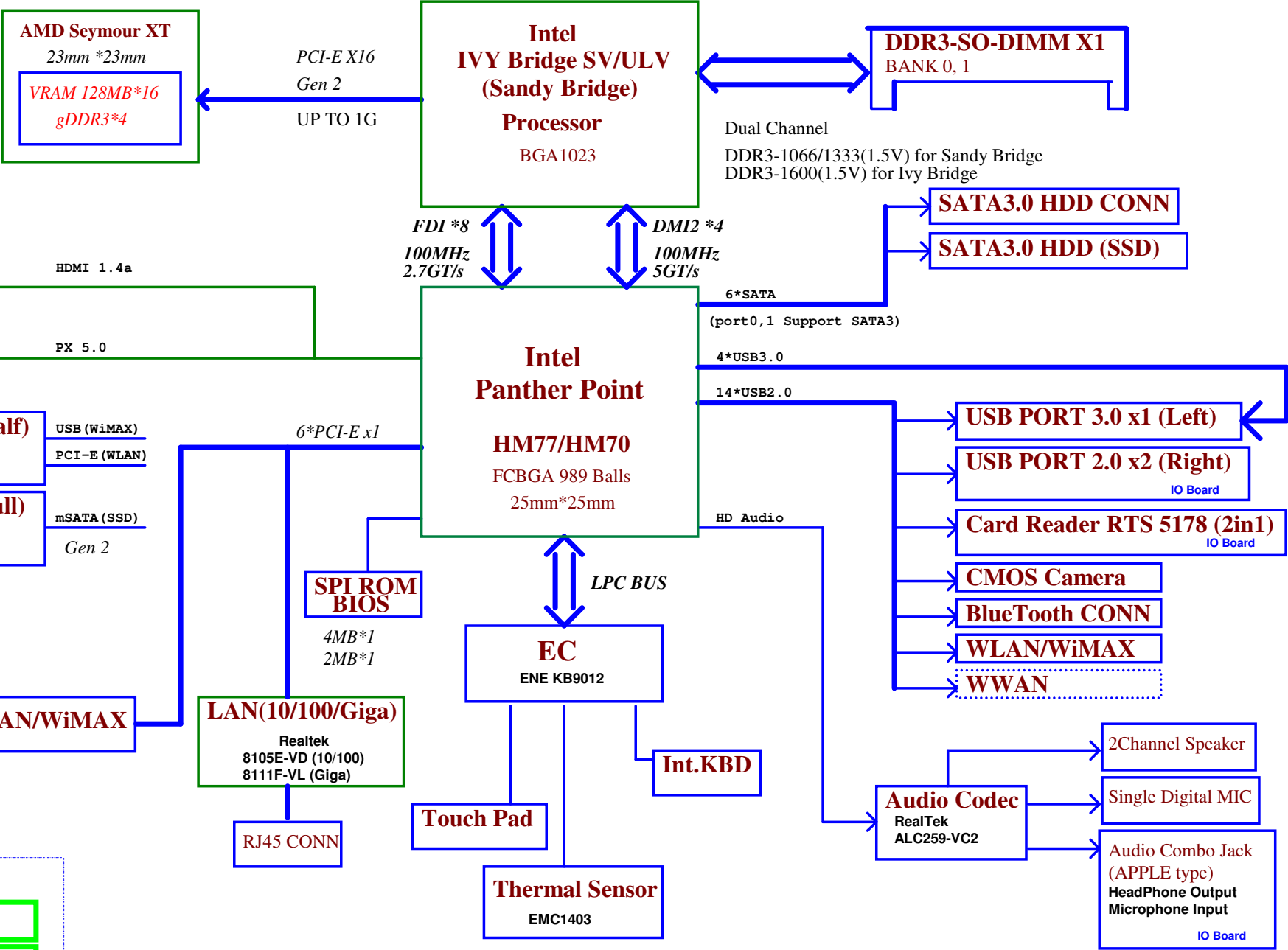
Intel Ivy Bridge ULV Processor + Panther Point PCH  
AMD Seymour XT

2011-12-28

REV : 0 . 1

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Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title Cover Page	
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# Chief River



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Issued Date	2011/07/21	Deciphered Date	2012/12/31	Title	MB Block Diagram
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Voltage Rails				
power plane	State	+B	+5VALW +3VALW	+1.5V +1.5V_IO +5VS +3VS +1.5VS +1.05VS_VTT +CPU_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS
S0				
S3				
S5 S4/AC				
S5 S4/ Battery only				
S5 S4/AC & Battery don't exist				

EC SM Bus1 address		EC SM Bus2 address	
Device	Address	Device	Address
Smart Battery	0001 011Xb	Thermal Sensor F75303M	1001_101xb

PCH SM Bus address	
Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

AMD-GPU SM Bus address	
Device	Address
Internal thermal sensor	1001 111Xb (0x9E)

SMBUS Control Table								
	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1	KB9012	X	V	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW					
SMB_EC_CK2	KB9012	X	X	X	X	X	X	V
SMB_EC_DA2	+3VALW							+3VS
SMBCLK	PCH	X	X	X	V	V	X	X
SMBDATA	+3VALW				+3VS	+3VS		
SML0CLK	PCH	X	X	X	X	X	X	X
SML0DATA	+3VALW							
SML1CLK	PCH	V	X	V	X	X	V	X
SML1DATA	+3VALW	+3VS		+3VS			+3VS	

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BOARD ID Table	
Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

USB 3.0	USB 2.0		Port	3 External USB Port
xHCI1	EHCI1	UHCI0	0	
xHCI2			1	USB 3.0 Port (Left Side)
xHCI3		UHCI1	2	Mini Card(WLAN)
xHCI4			3	
		UHCI2	4	X (USB PORT disabled on HM70 )
			5	X (USB PORT disabled on HM70 )
	EHCI2	UHCI3	6	X (USB PORT disabled on HM70 )
			7	X (USB PORT disabled on HM70 )
		UHCI4	8	USB/B (Right Side USB-BD)
			9	USB/B (Right Side USB-BD)
		UHCI5	10	USB Port (Right Side CR-BD)
			11	Camera (LVDS)
		UHCI6	12	X (USB PORT disabled on HM70 )
			13	X (USB PORT disabled on HM70 )

HM70 Disable xHCI3,xHCI4

	HM77	HM70	
SATA P0	GEN3/2/1	GEN3/2/1	SSD
SATA P1	GEN3/2/1	Disable	HDD (HM77)
SATA P2	GEN2/1	GEN2/1	HDD (HM70)
SATA P3	GEN2/1	Disable	
SATA P4	GEN2/1	GEN2/1	
SATA P5	GEN2/1	GEN2/1	

HM70 Disable P1,P3

BTO Item	BOM Structure
INTEL UMA only	UMA@
GPU:Seymour XT	PX@ PX5@
HDMI	HDMI@
HDD1 (HM77 SATA 3.0)	HDD1@
HDD2 (HM70 SATA 2.0)	HDD2@
Interna-Intel-USB3.0	IU3@
Interna-Intel-USB2.0	IU2@
Blue Tooth	BT@
10/100 LAN	8105E@
GIGA LAN	8111F@
Connector	ME@
45 LEVEL	45@
Unpop	@

	HM77	HM70	
PCie P1	Enable	Enable	LAN
PCie P2	Enable	Enable	WLAN
PCie P3	Enable	Enable	
PCie P4	Enable	Enable	
PCie P5	Enable	Disable	
PCie P6	Enable	Disable	
PCie P7	Enable	Disable	
PCie P8	Enable	Disable	

HM70 Disable P5,P6,P7,P8

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## Power-Up/Down Sequence

1. All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.

2. VDDR3 should ramp-up before or simultaneously with VDDC.

3. For LVDS, DPx\_VDD10 should ramp-up before DPx\_VDD18 and the PCIe Reference clock should begin before DPx\_VDD18. For power-down, DPx\_VDD18 should ramp-down before DPx\_VDD10.

4. The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD\_CT have ramped up.

5. VDDC and VDD\_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD\_CT starts to ramp-up (or vice versa).)

VDDR3(3.3VGS)

PCIE\_VDDC(1.0V)

VDDR1(1.5VGS)

VDDC/VDDCI(1.12V)

VDD\_CT(1.8V)

PERSTb

REFCLK

Straps Reset

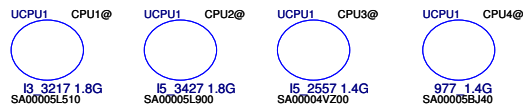
Straps Valid

Global ASIC Reset

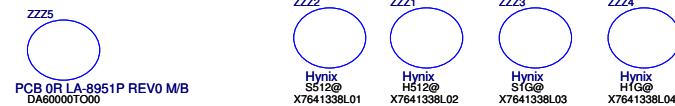
Note: Do not drive any IOs before VDDR3 is ramped up.

T4+16clock

## CPU part



## PCB part



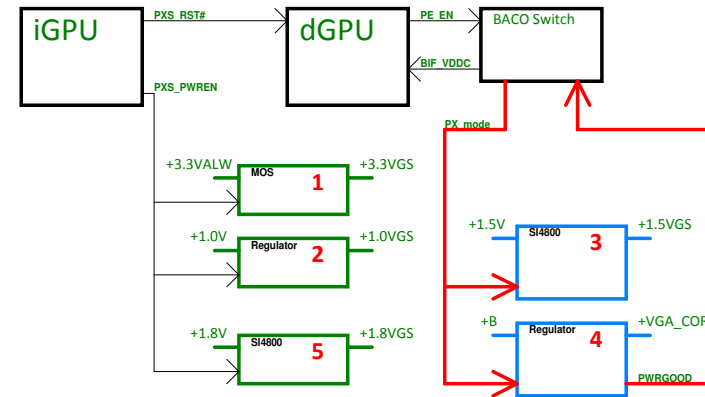
## Without BACO option :

PXS\_RST# : Low -> Reset dGPU ; High -> Normal operation  
PXS\_PWREN : Low -> dGPU Power OFF ; High -> dGPU Power ON

## BACO option :

PXS\_RST# : High -> Normal operation (dGPU is not reset on BACO mode)  
PXS\_PWREN : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode) BIF_VDDC=VGA_CORE When GPU enable BIF_VDDC=1.0V When BACO	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A



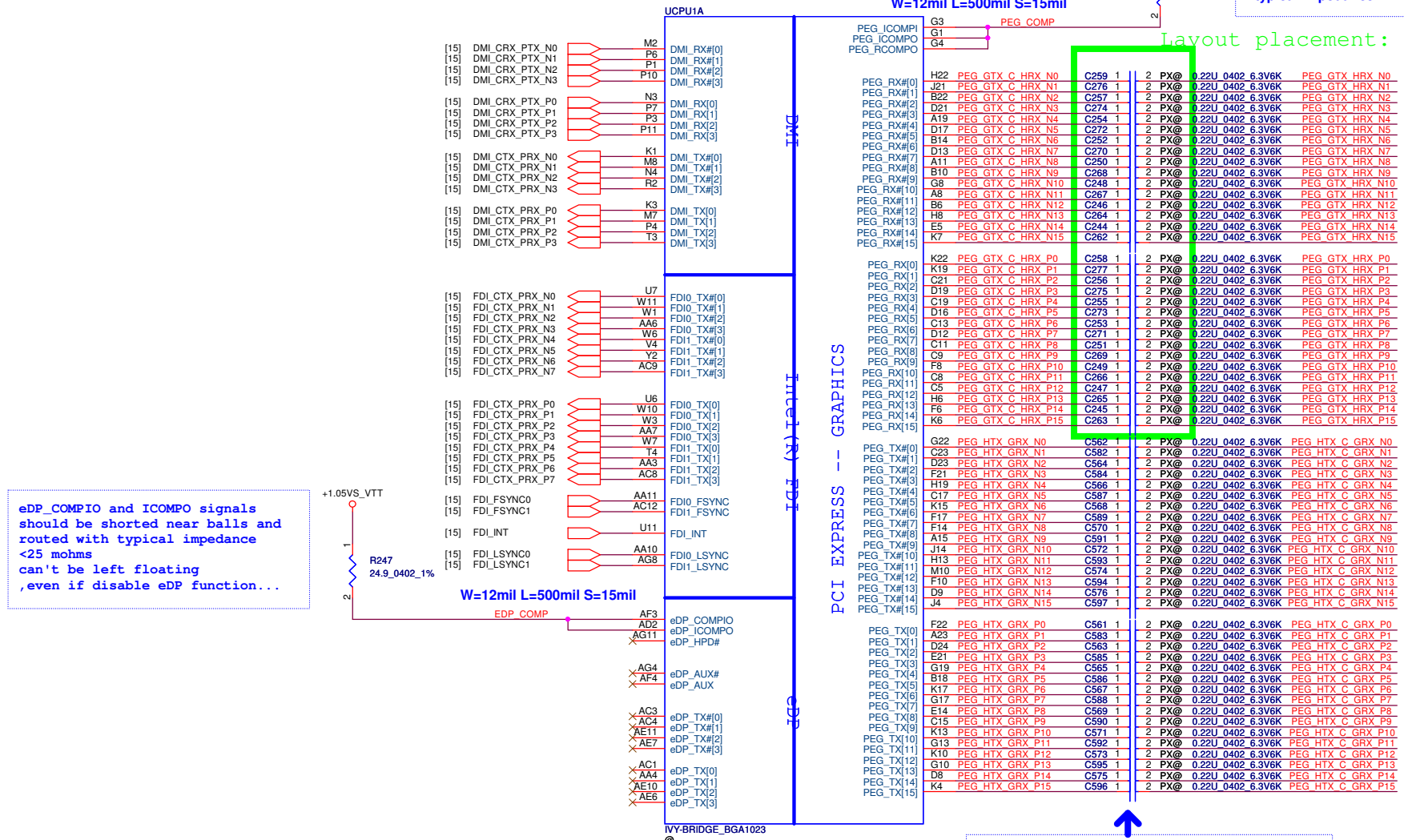
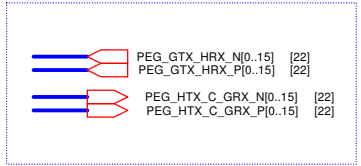
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eDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms, even if disable eDP function...

PEG\_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms  
PEG\_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

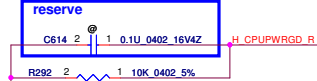
Layout placement: Place close to U8 (GPU)



Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIe Gen3 (8GT/s)

PCH->CPU  
UNCOREPWRGOOD:非CORE外的電OK  
SM\_DRAMPWROK:DRAM power ok  
RESET#:都ok後請CPU做reset

Follow DG 1.5& Tacoma\_Fall2 1.0



UNCOREPWRGOOD:非CORE外的電OK

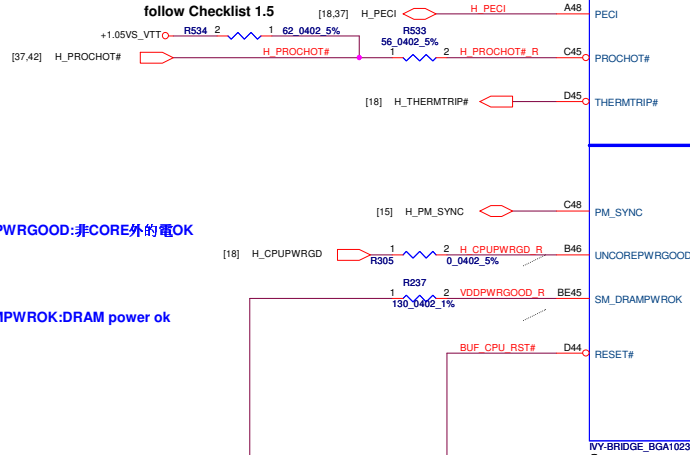
SM\_DRAMPWROK:DRAM power ok

PROC\_SELECT#  
PH VCPLL and connect to PCH DF\_TV5

偵測CPU有無安裝

XBOX 三紅功能

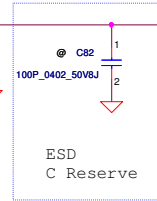
follow Checklist 1.5



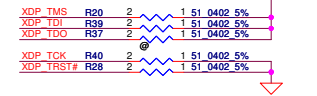
Checklist1.5 P.67 Graphis Disable Guide  
DIS only SKU eDP disable  
DPLL\_REF\_SSCLK PD 1K\_5% to GND  
DPLL\_REF\_SSCLK# PH 1K\_5% to +1.05VS\_VTT

SM\_RCOMP0,SM\_RCOMP1  
W=20mil L=500mil S=13mil  
SM\_RCOMP2  
W=15mil L=500mil S=13mil

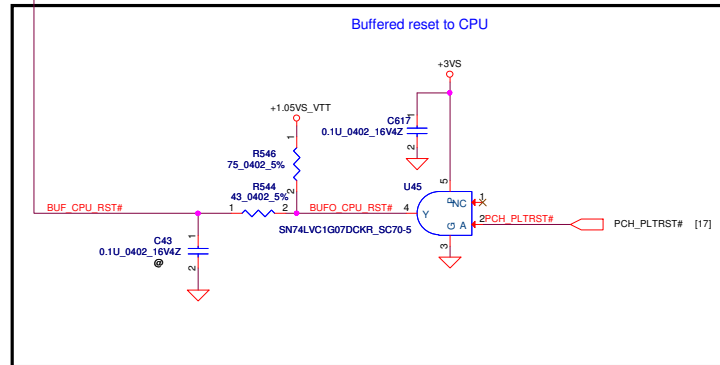
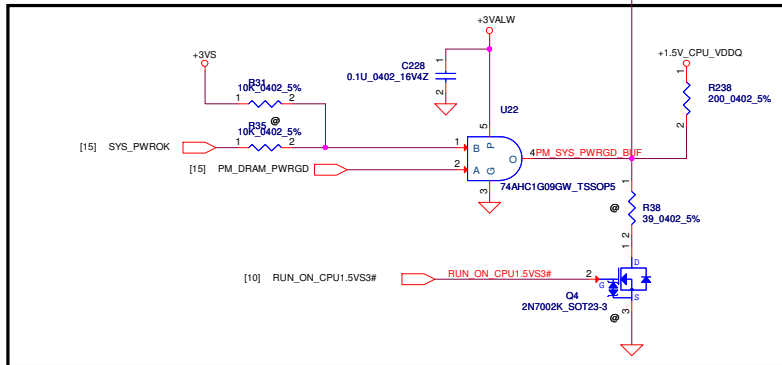
DDR3 Compensation Signals



PU/PD for JTAG signals



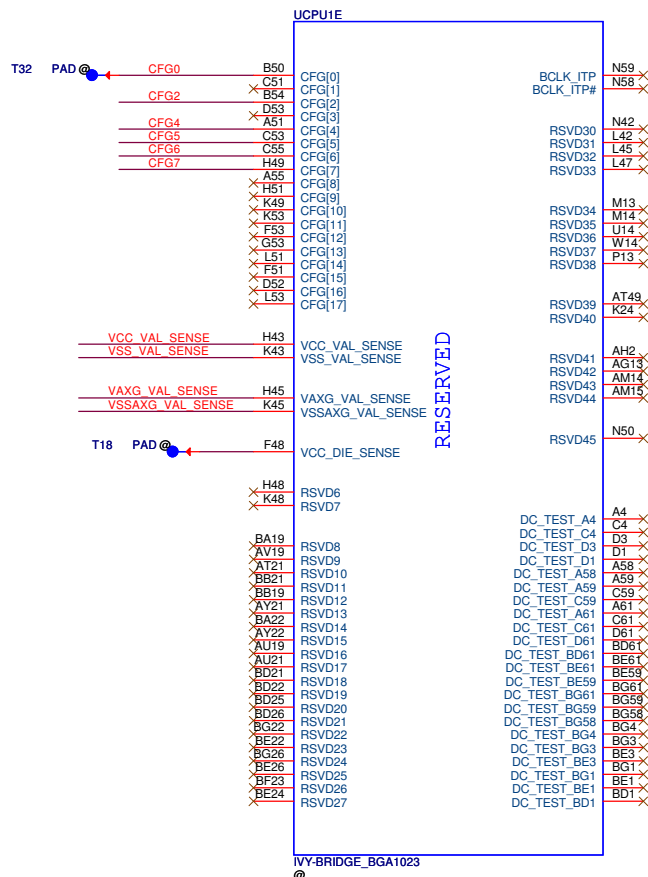
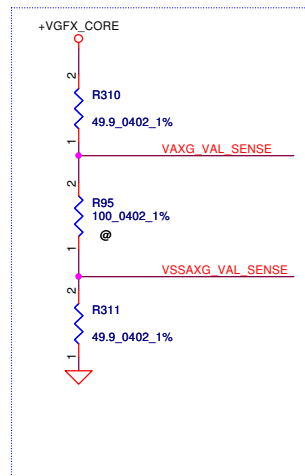
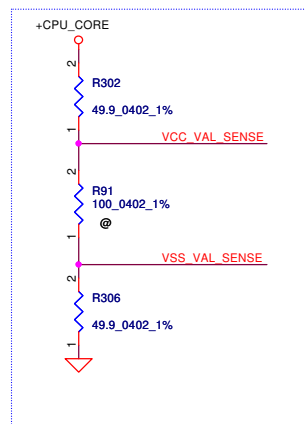
Tacoma\_Fall2 1.0 PH 1K +3VS  
Check list 1.5 PH 1K +3VS  
Debug port DG1.1-1.3 50-5K ohm



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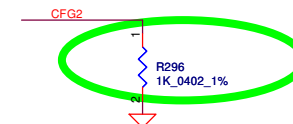




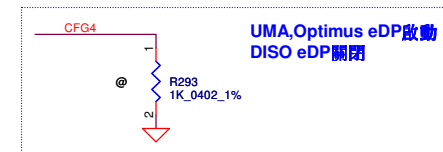


These pins are for solder joint reliability and non-critical to function. For BGA only.

## CFG Straps for Processor

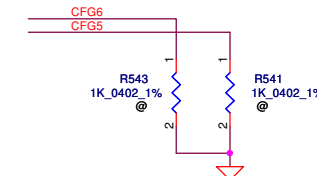


PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition ★ 0: Lane Reversed

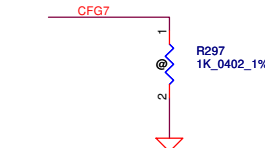


UMA,Optimus eDP啟動  
DISO eDP關閉

eDP enable	
CFG4	★ 1: Disable 0: Enable



PCIe Port Bifurcation Straps	
CFG[6:5]	★ 11: (Default) 1x16 PCI Express 10: 2x8 PCI Express 01: Reserved 00: 1x8,2x4 PCI Express



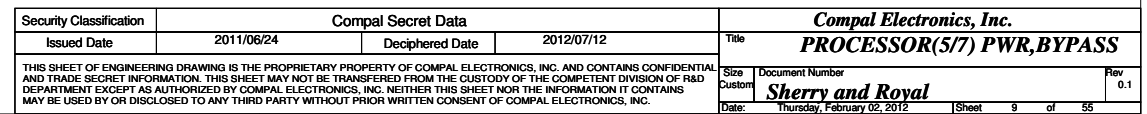
PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Tacoma\_Fall12 1.0 P.12

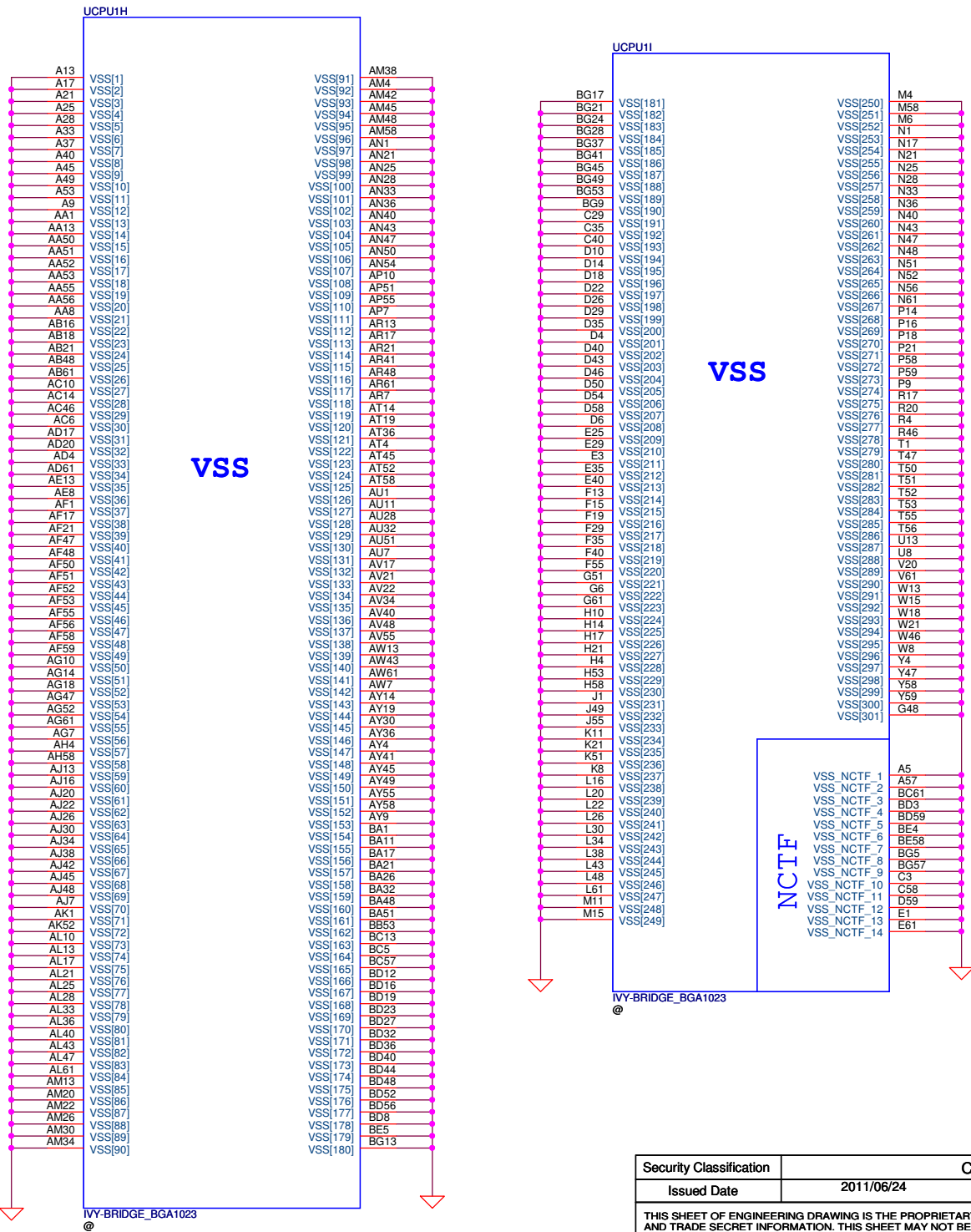
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Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title	PROCESSOR(4/7) RSVD,CFG
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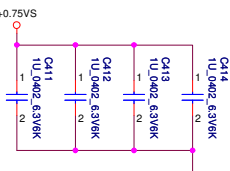
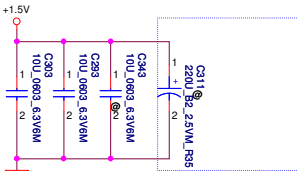
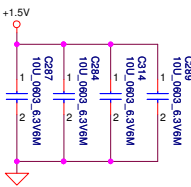
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Issued Date		2011/06/24		Deciphered Date		2012/07/12		Title			
								PROCESSOR(7/7) VSS			
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DDR_A_DQS#[0..7]	[7]
DDR_A_DQS[0..7]	[7]
DDR_A_D[0..63]	[7]
DDR_A_MA[0..15]	[7]

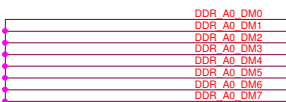
The circuit diagram shows a +1.5V DC voltage source connected to four parallel branches. Each branch contains a capacitor component:

- Branch 1: Capacitor C394, value 1U\_0402\_6.3V6K.
- Branch 2: Capacitor C396, value 1U\_0402\_6.3V6K.
- Branch 3: Capacitor C391, value 1U\_0402\_6.3V6K.
- Branch 4: Capacitor C310, value 1U\_0402\_6.3V6K.

All capacitors are connected between the +1.5V supply rail and a common ground rail.



DDR A0 DM0
DDR A0 DM1
DDR A0 DM2
DDR A0 DM3
DDR A0 DM4
DDR A0 DM5
DDR A0 DM6
DDR A0 DM7



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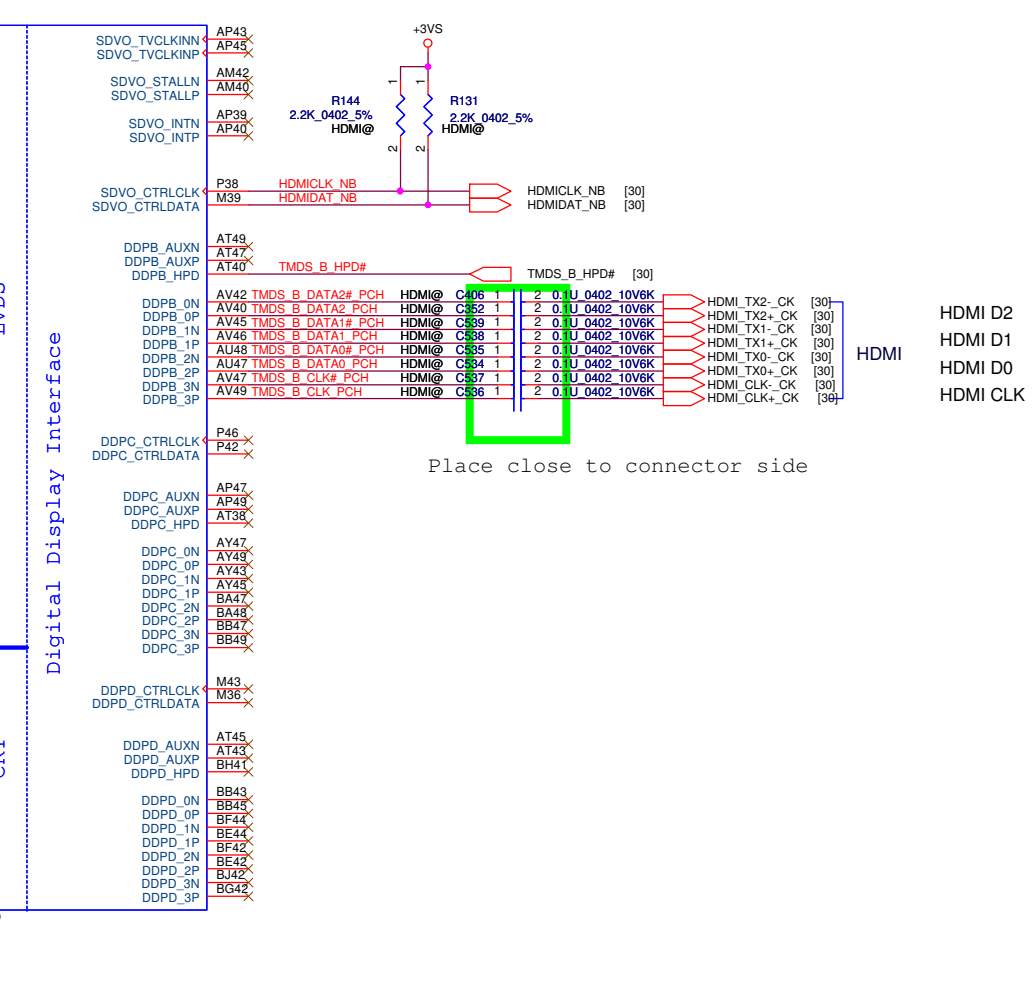
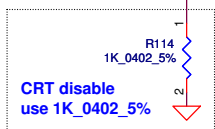
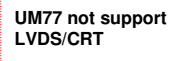






LVDS disable:  
DATA/Clock/Control an NC  
VCC TX LVDS.VCCA LVDS PD to GND

**CRT disable:**  
**DATA/Clock/Control an NC**  
**VCCADAC connect to +3VS**  
**DAC IREF connect 1K 0402 5%**



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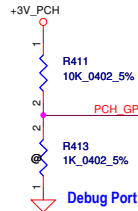


# HDA\_SYNC PH(PLL =+1.5VS)

## GPIO28

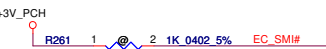
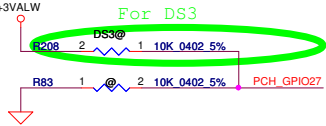
### On-Die PLL Voltage Regulator

This signal has a weak internal pull up  
 \* H : On-Die PLL voltage regulator enable  
 L : On-Die PLL Voltage Regulator disable

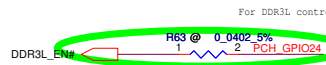
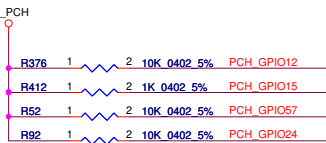
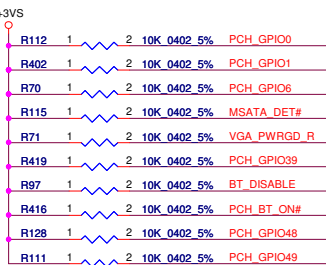


Debug Port DG 1.2 PH 4.7K +3VALW\_PCH

Deep S4,S5 wake event signal  
 RTC alarm,Power BTN,GPIO27  
 PCH\_GPIO27 (Have internal Pull-High)  
 Deep S4,S5 wake event signal



SATA2GP/GPIO36 & SATA3GP/GPIO37  
 Sampled at Rising edge of PWROK.  
 Weak internal pull-down.  
 (weak internal pull-down is disabled  
 after PLTRST# de-asserts)  
 NOTE: This signal should NOT be  
 pulled high when strap is sampled

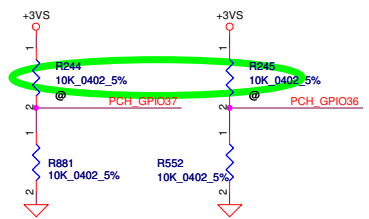


GPIO24 Unmuxplexed  
 NOTE: GPIO24 configuration  
 register bits are not cleared by  
 CF9h reset event.  
 CRB1.0 PH10K to +3VALW

Fan Tachometer Inputs  
 TACH1~7 only on server  
 can insted to GPIO

No use PH 10K +3VS	PCH_GPIO0	T7
No use PH 10K +3VS	PCH_GPIO1	A42
No use PH 10K +3VS	PCH_GPIO6	H36
No use PH 10K +3VALW	[37] EC_SCI#	E38
No use PH 10K +3VALW	[37] EC_SMI#	C10
No use PH +3VALW	PCH_GPIO12	C4
No use PH +3VALW	[37] EC_LID_OUT#	G2
No use PH +3VS	[31] mSATA_DET#	U2
No use PH +3VS	[22,49] VGA_PWRGD	D40
No use PH 10K +3VS	[31] BT_DISABLE	T5
No use PH +3VALW	PCH_GPIO24	E8
No use PD 10K to GND	EC_LID_OUT#	E16
No use PH 10K +3VALW	PCH_GPIO28	P8
No use PH 10K +3VS	[31] PCH_BT_ON#	K1
No use can NC	R243	K4
Can't PH	PCH_GPIO36	V8
Can't PH	PCH_GPIO37	M5
No use PH 10K +3VS	OPTIMUS_EN#	N2
No use PH 10K +3VS	PCH_GPIO39	M3
No use PH 10K +3VS	PCH_GPIO48	V13
SATA5GP&TEMP_ALERT# CRB PH 10K +3VS	PCH_GPIO49	V3
No use PH +3VALW	PCH_GPIO57	D6

UMA@	OPTIMUS_EN#
PX@	
	GPIO38
	OPTIMUS_EN#
	0
	1



GPIO36/GPIO37 is Strap functionality  
 that requires internal pull down to be sampled at rising PWROK.  
 When uses as SATA2GP/SATA3GP for mechanical presence detect  
 -use a external pull up 150K-200K ohm to Vcc3\_3  
 When used as GP input  
 -ensure GPI is not driven high during strap sampling window  
 When Unused as GPIO or SATA\*GP  
 -use 8.2K-10K pull-down  
 check list page 47

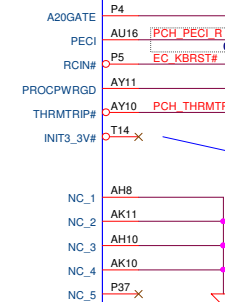
U13F	BMBUSY# / GPIO0	T7
	TACH1 / GPIO1	A42
	TACH2 / GPIO6	H36
	TACH3 / GPIO7	E38
	GPIO8	C10
	LAN_PHY_PWR_CTRL / GPIO12	C4
	GPIO15	G2
	SATA4GP / GPIO16	U2
	TACH0 / GPIO17	D40
	SCLOCK / GPIO22	T5
	GPIO24 / MEM_LED	E8
	GPIO27	E16
	GPIO28	P8
	STP_PC# / GPIO34	K1
	GPIO35	K4
	SATA2GP / GPIO36	V8
	SATA3GP / GPIO37	M5
	SLOAD / GPIO38	N2
	SDATAOUT0 / GPIO39	M3
	SDATAOUT1 / GPIO48	V13
	SATA5GP / GPIO49	V3
	GPIO57	D6

A4	VSS_NCTF_1
A44	VSS_NCTF_2
A45	VSS_NCTF_3
A46	VSS_NCTF_4
A5	VSS_NCTF_5
A6	VSS_NCTF_6
B3	VSS_NCTF_7
B47	VSS_NCTF_8
BD1	VSS_NCTF_9
BD49	VSS_NCTF_10
BE1	VSS_NCTF_11
BE49	VSS_NCTF_12
BF1	VSS_NCTF_13
BF49	VSS_NCTF_14

PANTHER\_FCBGA989  
 <BOM Structure>

GPIO  
 CPU/MISC  
 NCTF

C40	PCH_GPIO68
B41	PCH_GPIO69
C41	PCH_GPIO70
A40	PCH_GPIO71



BG2	VSS_NCTF_15
BG48	VSS_NCTF_16
BH3	VSS_NCTF_17
BH47	VSS_NCTF_18
BJ4	VSS_NCTF_19
BJ44	VSS_NCTF_20
BJ45	VSS_NCTF_21
BJ46	VSS_NCTF_22
BJ5	VSS_NCTF_23
BJ6	VSS_NCTF_24
C2	VSS_NCTF_25
C48	VSS_NCTF_26
D1	VSS_NCTF_27
D49	VSS_NCTF_28
E1	VSS_NCTF_29
E49	VSS_NCTF_30
F1	VSS_NCTF_31
F49	VSS_NCTF_32

INIT3\_3V Checklist1.5 P.69  
 This signal has weak internal  
 PU, can't pull low,leave NC

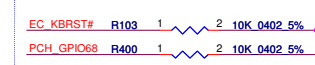
TS\_VSS1~4  
 PD to GND

9/15 Layout  
 request remove  
 Test point  
 They will route  
 by itself

PCH_GPIO70	Function
0	13/14"
1	NA
PCH_GPIO71	Function
0	USB3.0 by PCH
1	USB3.0 by NEC

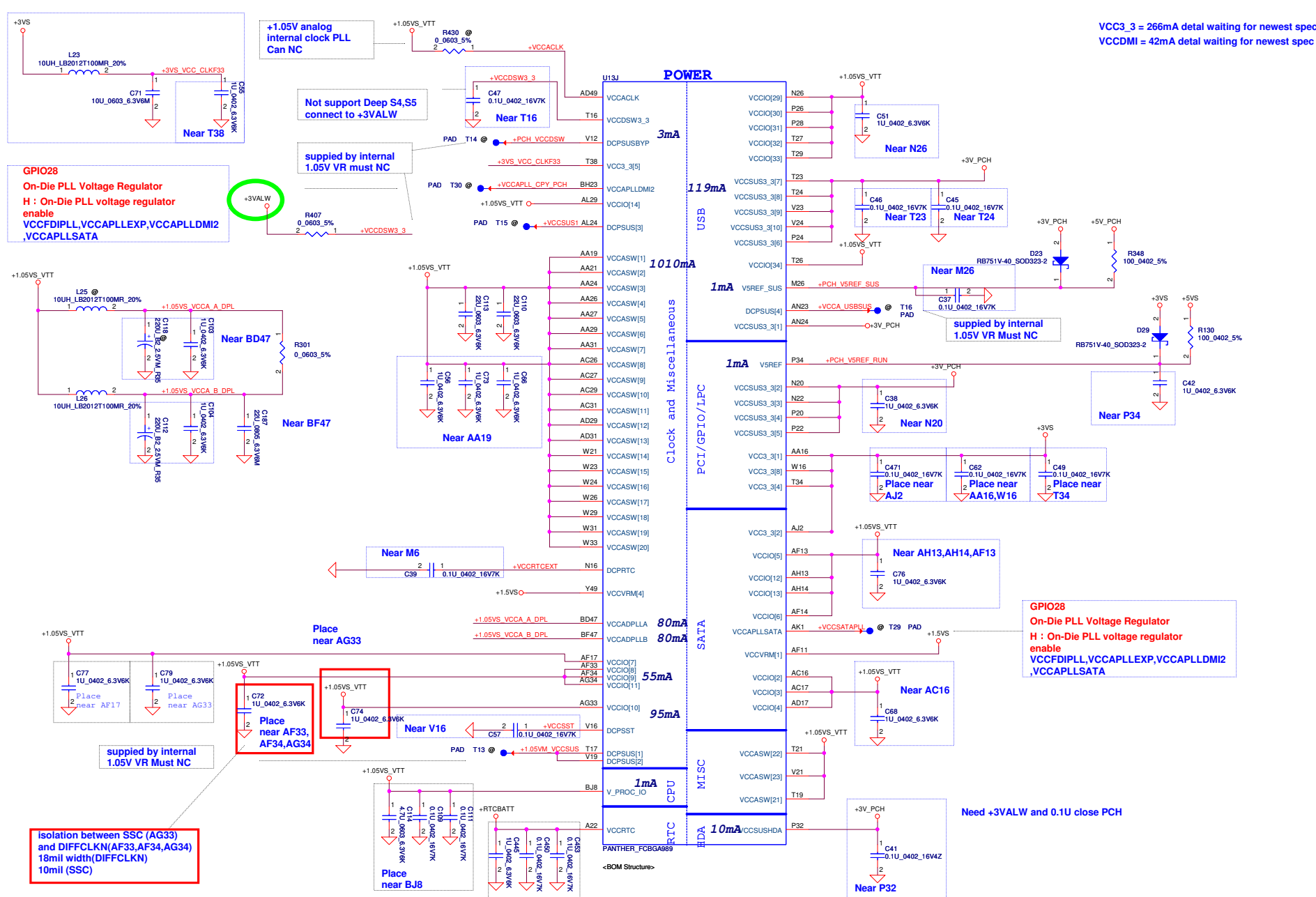
Need?

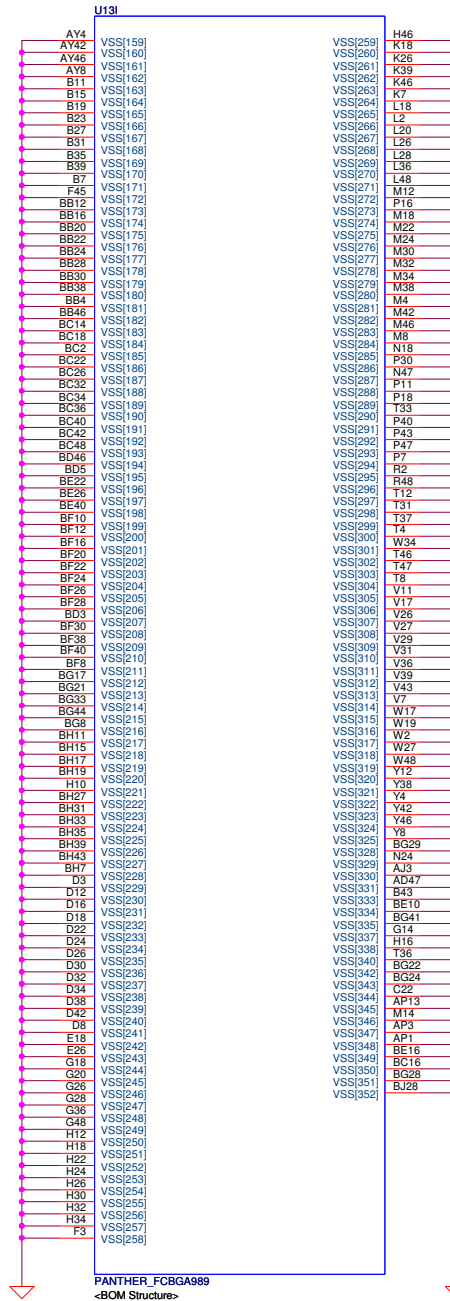
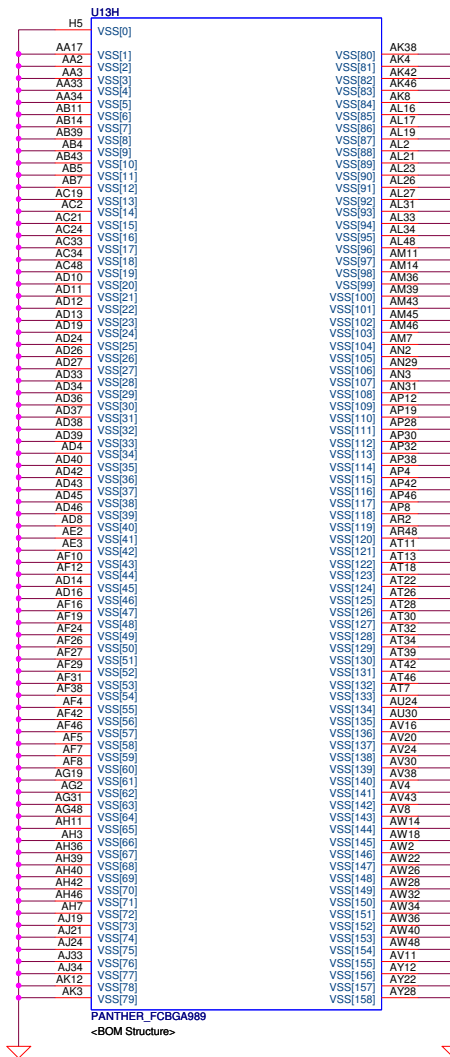
PECI CPU-EC  
 CTRL+ALT+DEL  
 non CPU power ok  
 130c shut down



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		Date	Thursday, February 02, 2012
		Sheet	18 of 55





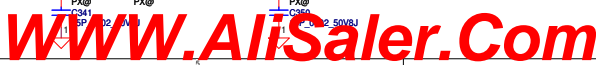


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				Sherry and Royal	0.1
				Date: Thursday, February 02, 2012	Sheet 21 of 55



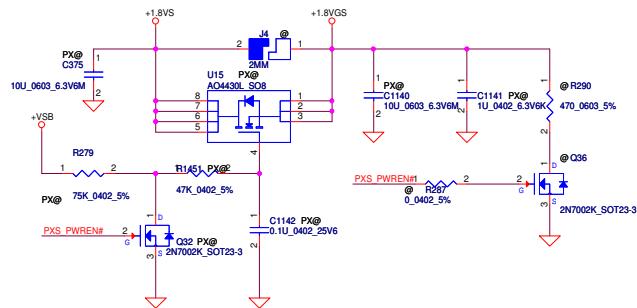




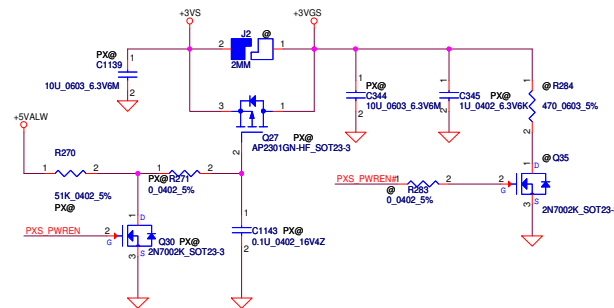


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				SeymourXT-S3 Main Generic/MSIO			
				Size C		Document Number	
Date:				Thursday, February 02, 2012		Sheet 23 of 55	

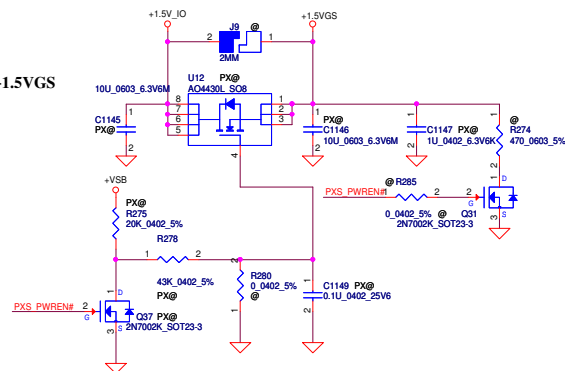
### +1.8VS TO +1.8VGS



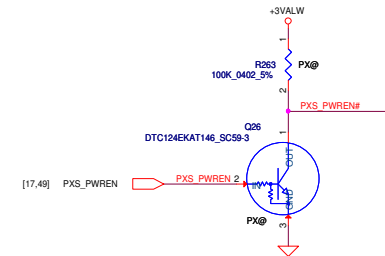
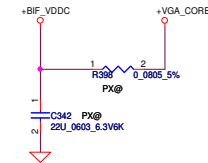
### +3.3VS TO +3.3VGS



### +1.5V TO +1.5VGS

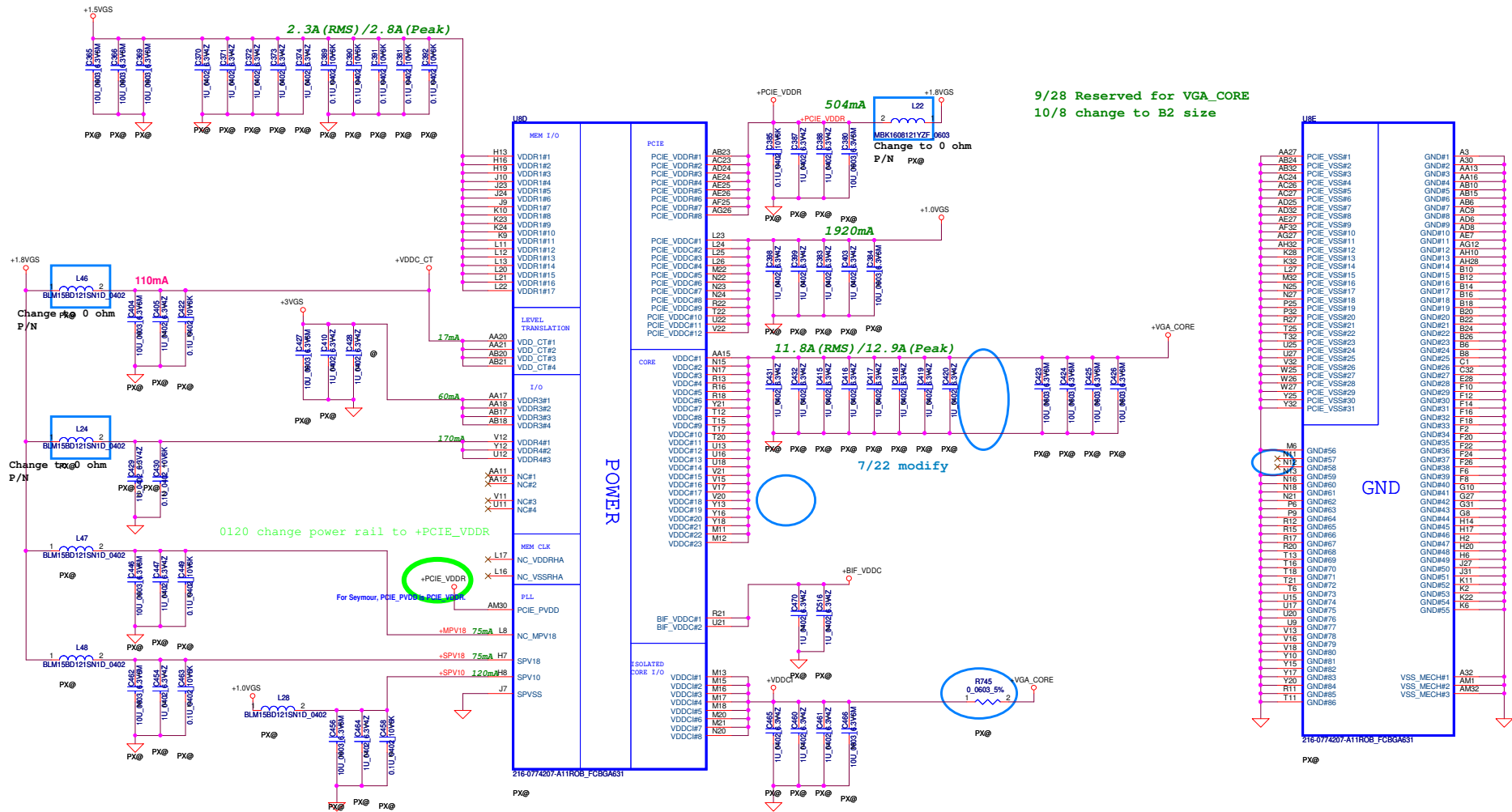


55mA@1.0V, in BACO mode



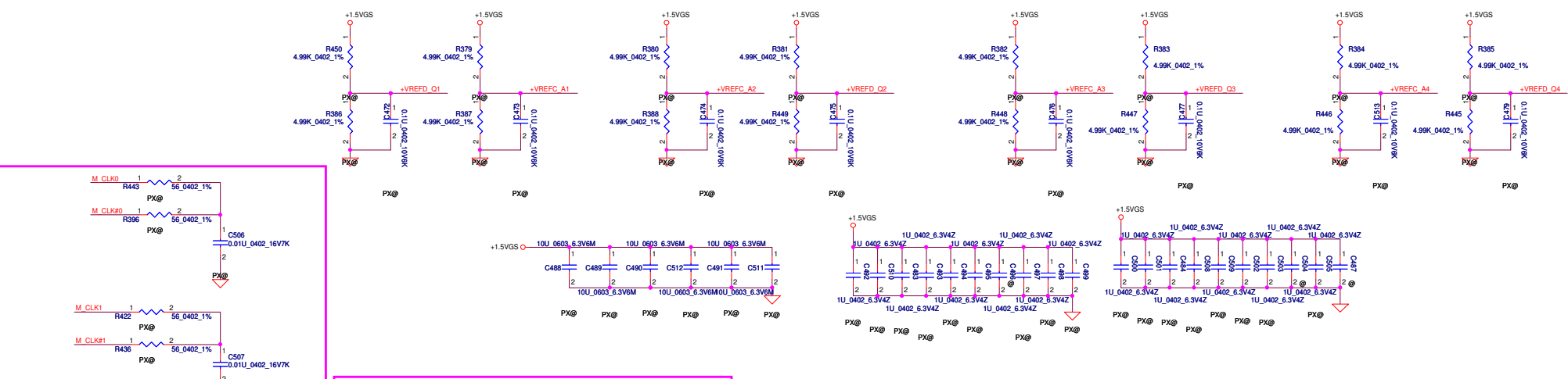
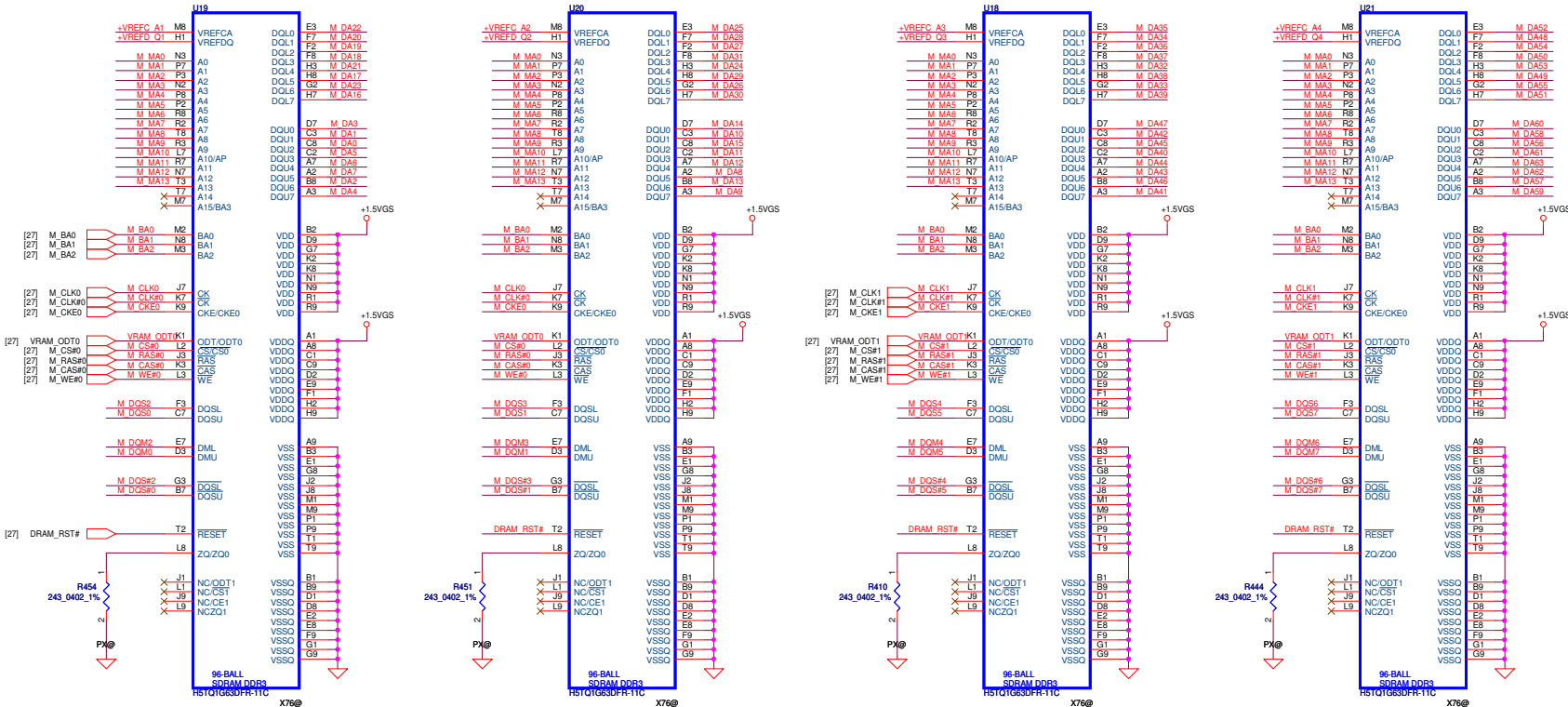
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Size	C	Document Number	Sherry and Royal	Rev
Date:	Thursday, February 02, 2012	Sheet	24	of 55







[27] M\_DA[63..0] M\_DA[63..0]  
[27] M\_MA[13..0] M\_MA[13..0]  
[27] M\_DQM[7..0] M\_DQM[7..0]  
[27] M\_DQS[7..0] M\_DQS[7..0]  
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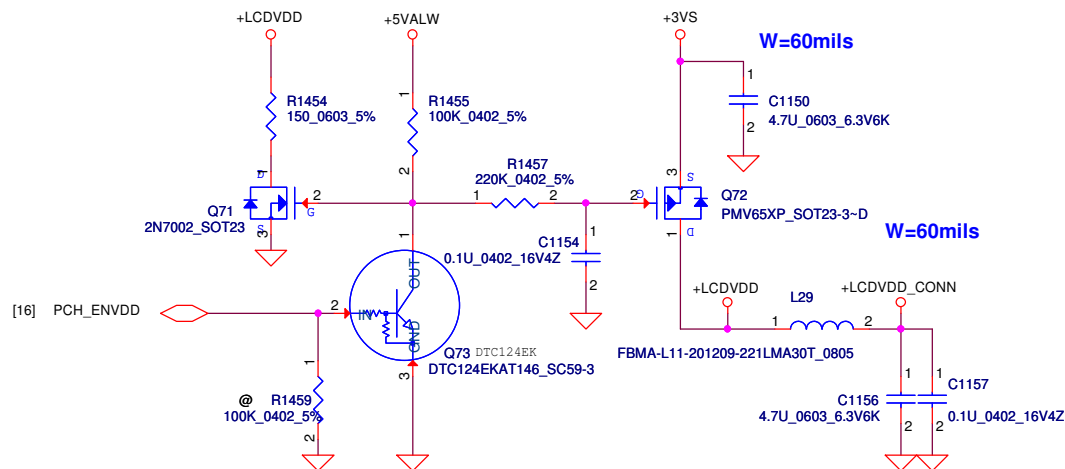


ref 139-02 recommend  
add off page  
Park SCL recommend pu 60.4 ohm  
VRAM P/N :  
Hynix : SA000041S10 (S IC D3 64MX16 H5TQ1G63BFR-11C FBGA C38! )  
Samsung : SA000041T10 (S IC D3 64MX16 K4W1G1646E-HC11 FBGA C38! )  
update VRAM P/N : 0619 update

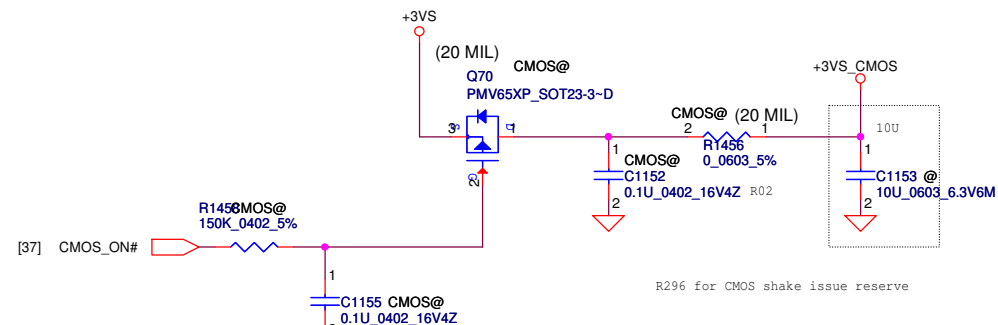
WWW.AliSaler.Com

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Size	C	Document Number	Rev 0.1
Date	Thursday, February 02, 2012	Sheet	28 of 55

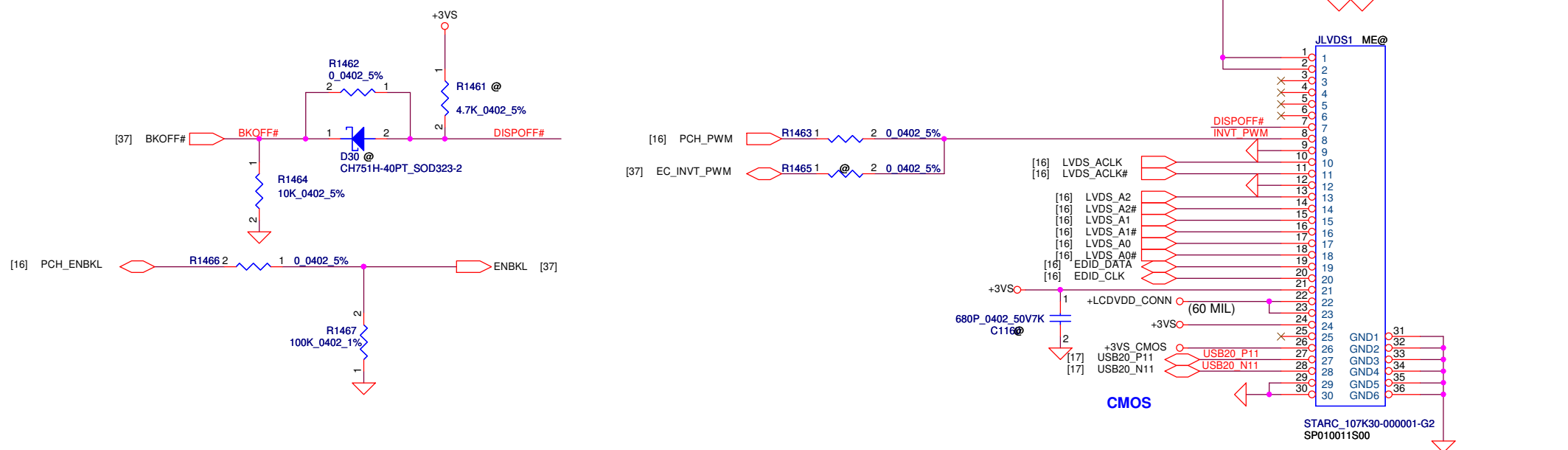
# LCD POWER CIRCUIT



# CMOS Camera



# VGA LCD/PANEL BD. Conn.



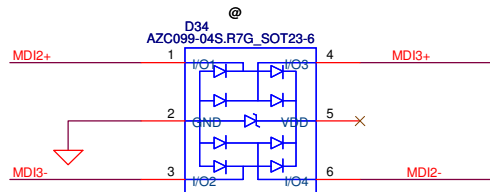
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Size		Document Number		Sherry and Royal	
Date:		Thursday, February 02, 2012		Rev 0.1	
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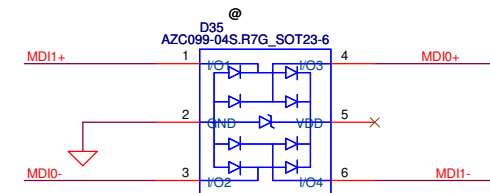






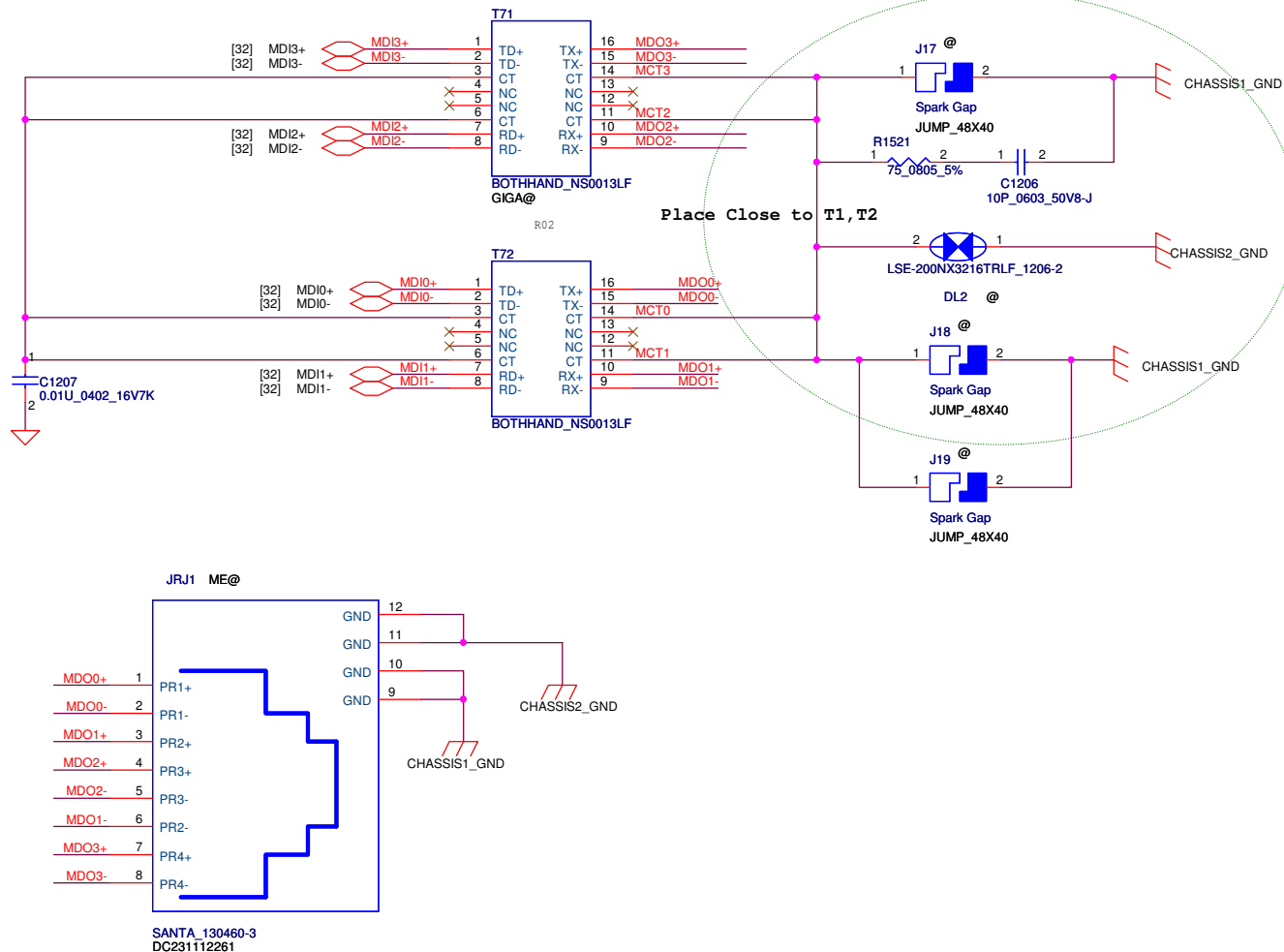


Place Close to T71



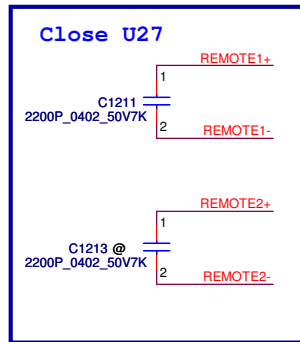
Place Close to T72

D34/D35  
1'S PN:SC300001G00  
2'S PN:SC300002E00

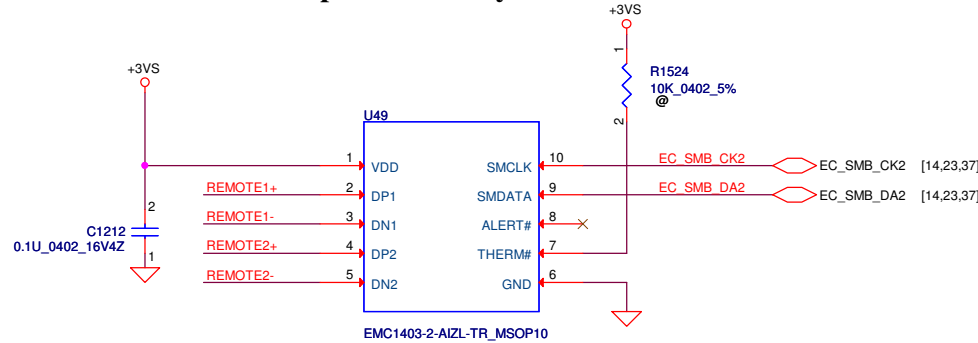


Reserve for EMI go rural solution

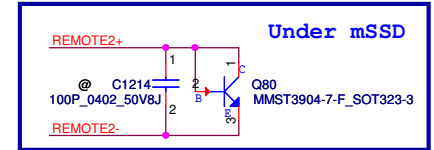
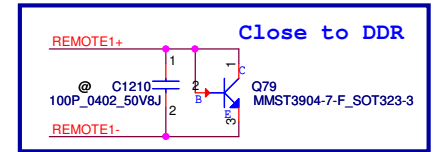
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				Size	Document Number	Rev
				Sherry and Royal		0.1
Date:		Thursday, February 02, 2012		Sheet	33	of 55



## SMSC thermal sensor placed near by VRAM

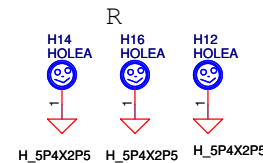
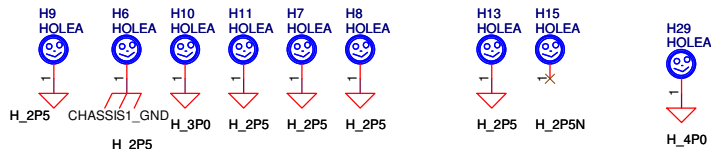
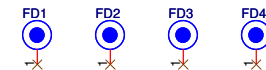
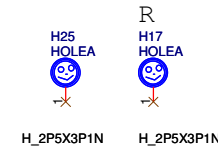
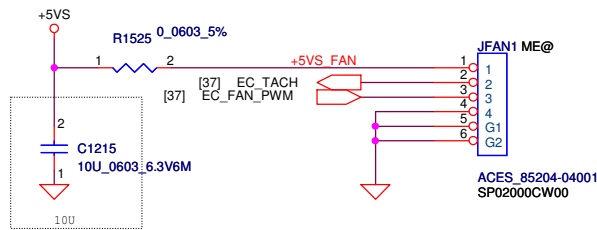


Address 1001\_101xb



REMOTE1,2+/-:  
Trace width/space:10/10 mil  
Trace length:<8"

## FAN1 Conn



M/B 橢圓孔 M/B KB 橢圓孔

A  
2P5 \* 9 pcd

F G

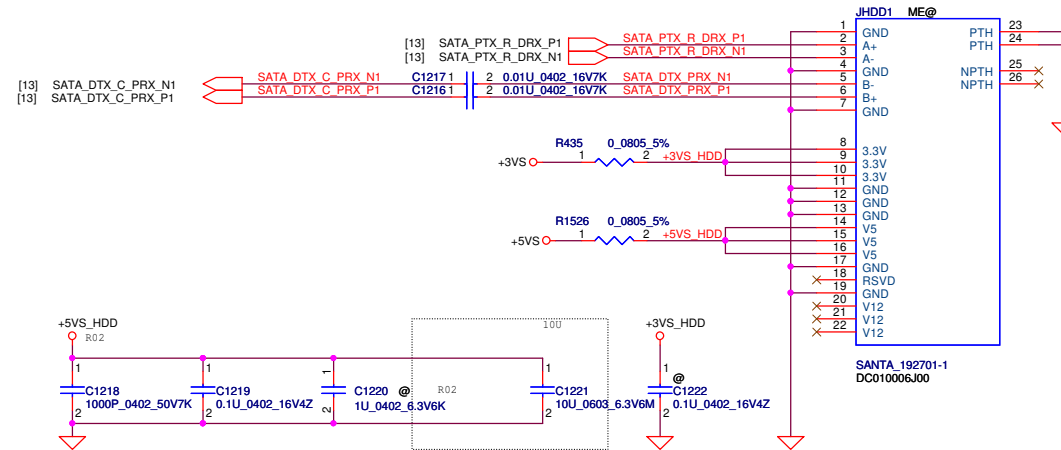
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					Date: Thursday, February 02, 2012	Sheet 34 of 55

B CPU

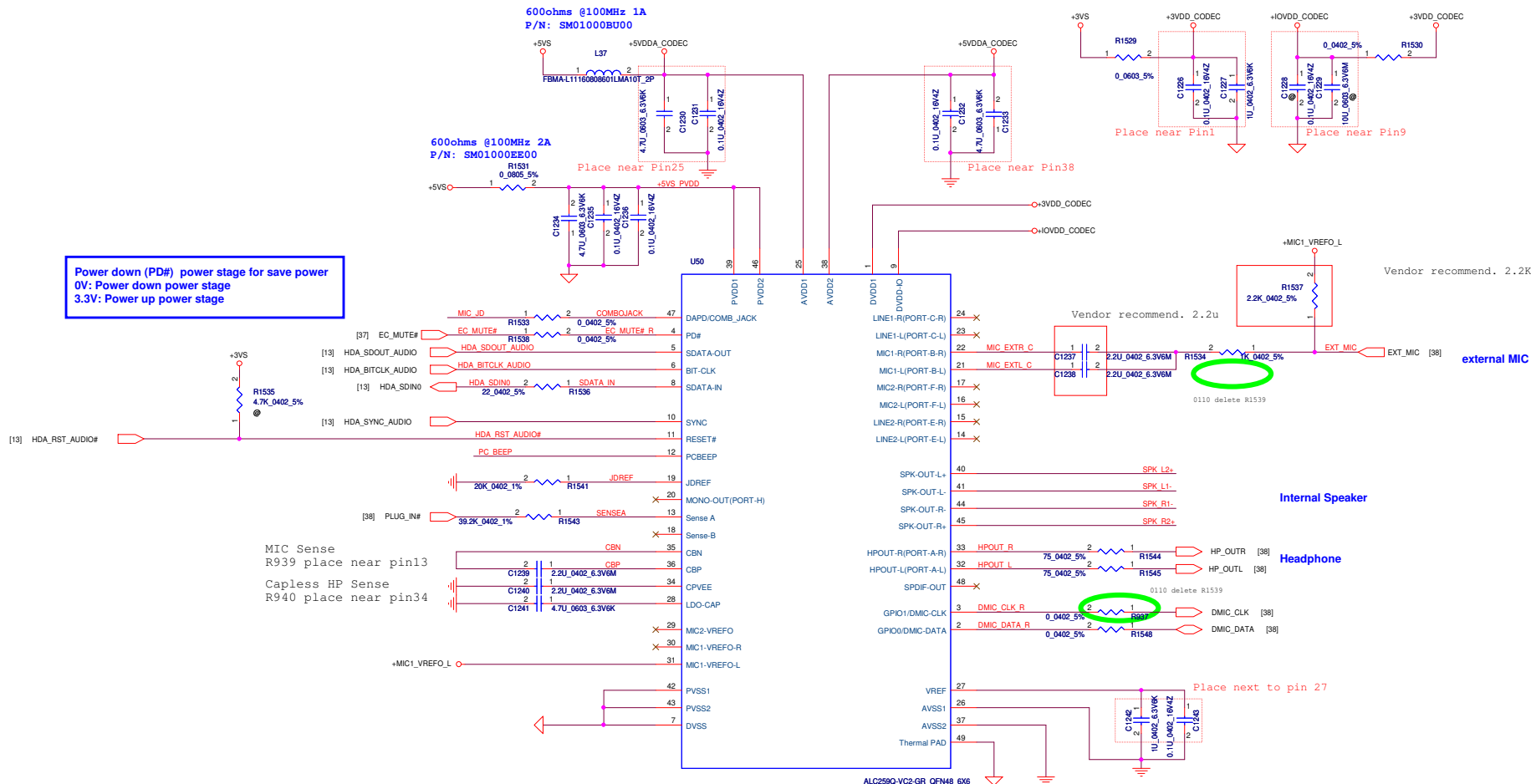
C GPU

D LAN

# SATA HDD Conn.



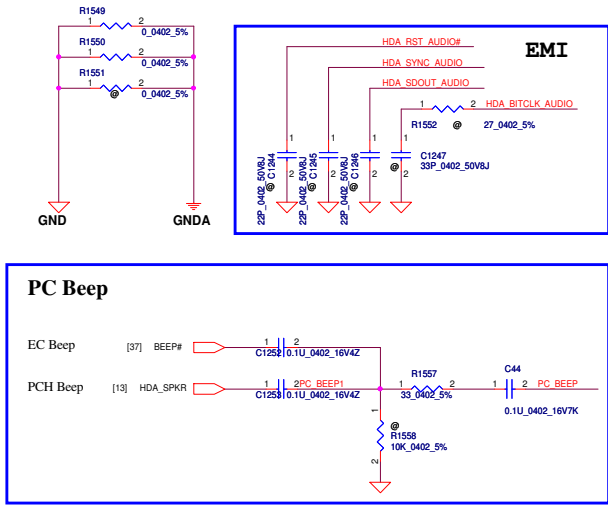
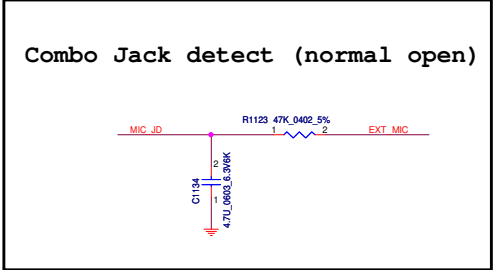
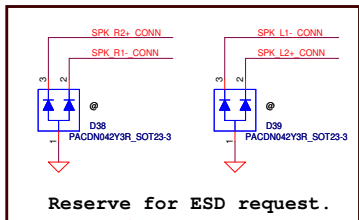
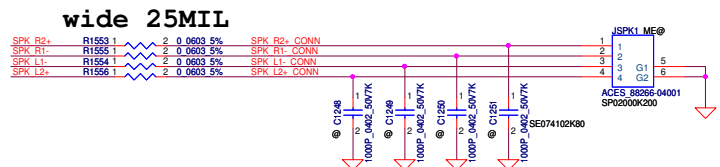
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				Size	Rev
				Custom	0.1
				Sherry and Royal	
				Date: Thursday, February 02, 2012	Sheet 35 of 55



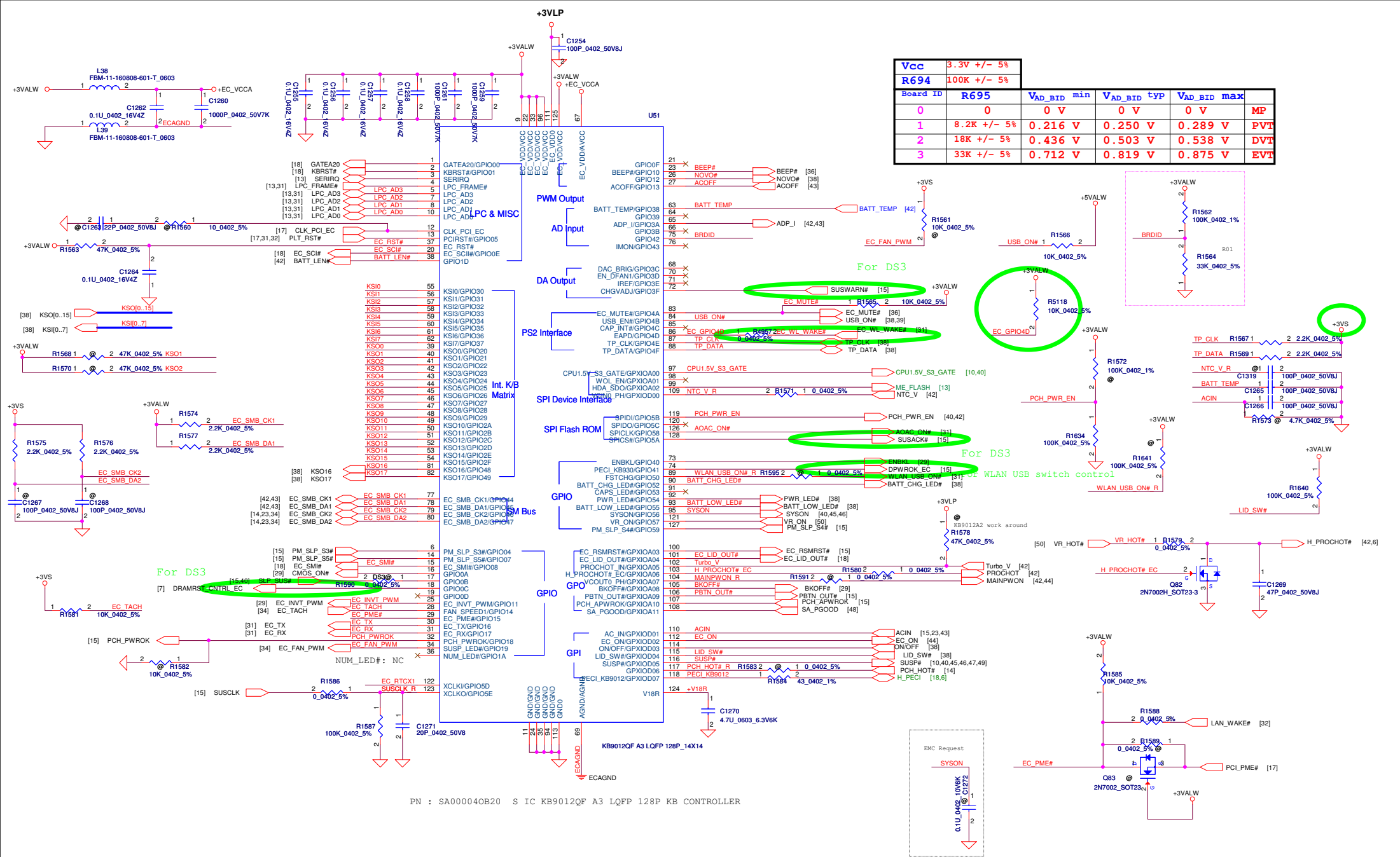
Power down (PD#) power stage for save power  
0V: Power down power stage  
3.3V: Power up power stage

MIC Sense  
R939 place near pin13  
Capless HP Sense  
R940 place near pin34

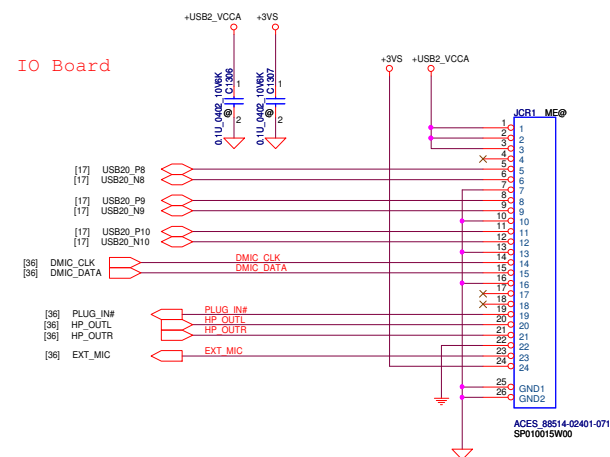
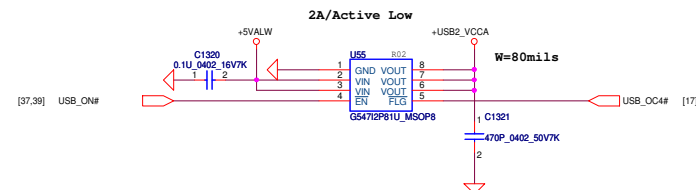
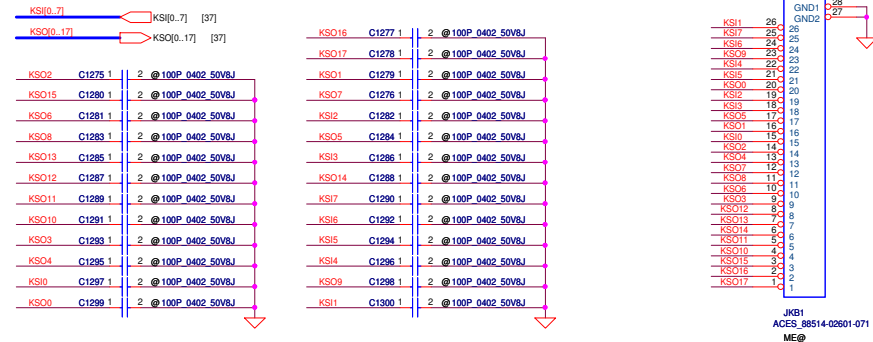
Pin Assignment	Location	Function
SPK-OUT (Pin40/41/44/45)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
MIC1 (Pin21/22)	External	Mic in

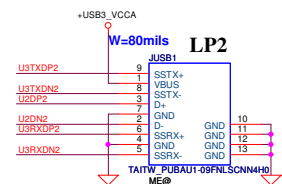
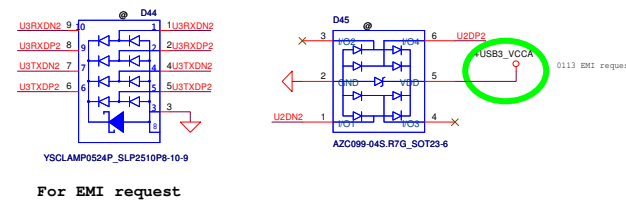
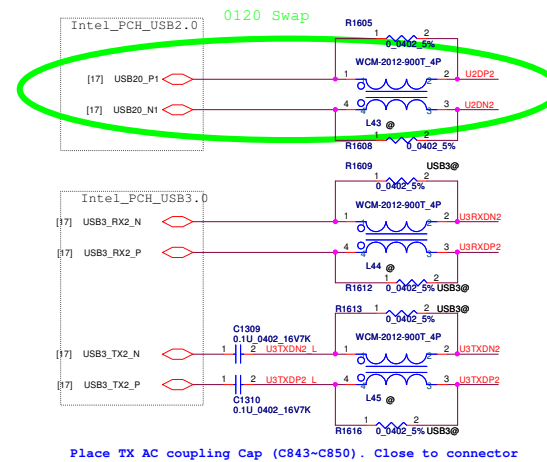
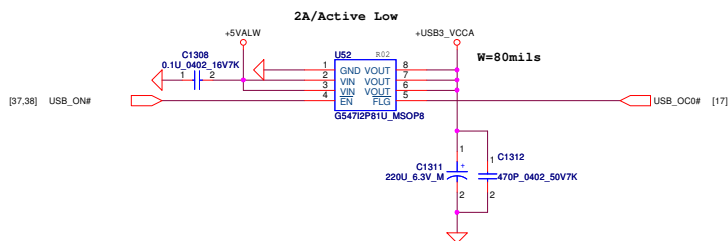






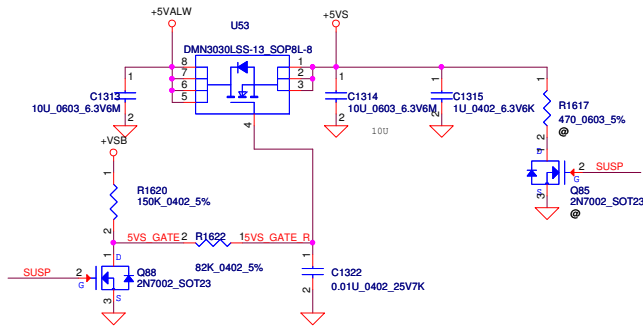
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				<b>Sherry and Royal</b>		
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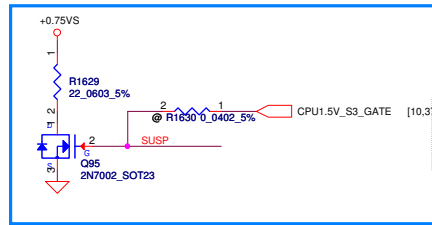
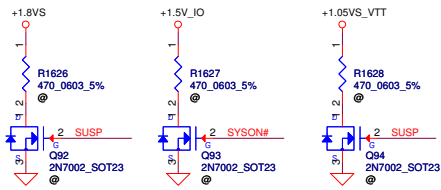
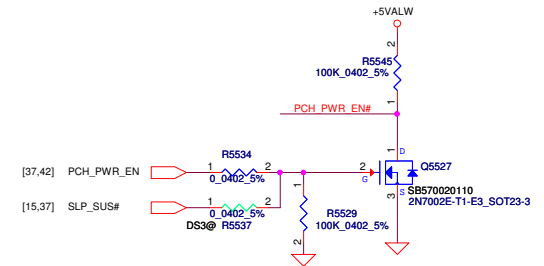
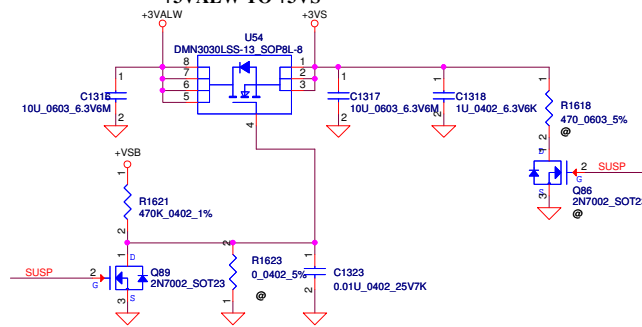


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### +5VALW TO +5VS

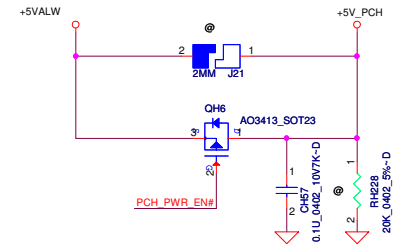
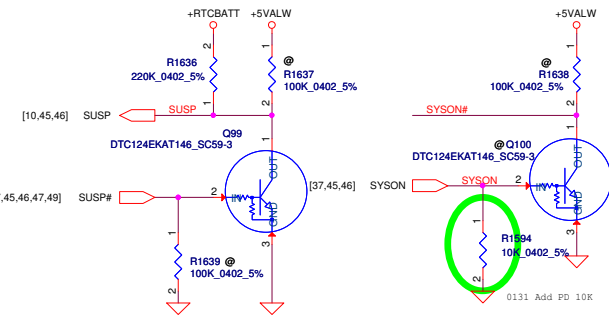
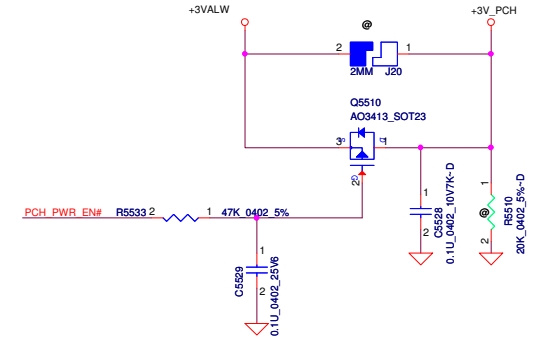
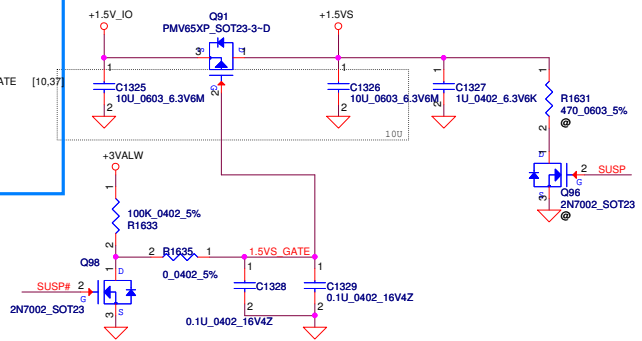


### +3VALW TO +3VS

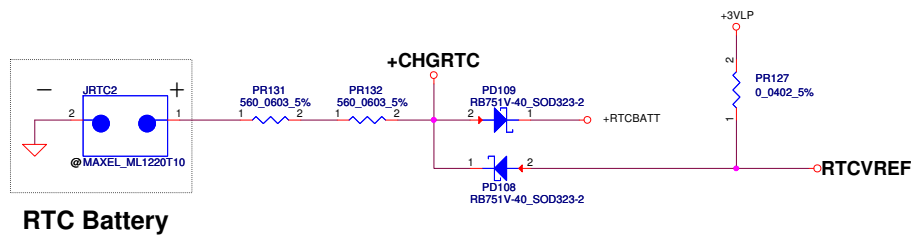
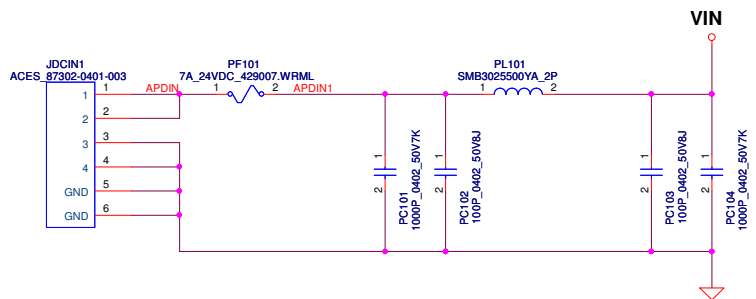


For Intel S3 Power Reduction.

### +1.5V\_IO to +1.5VS

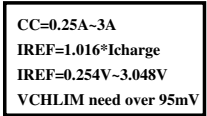


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				DC Interface			
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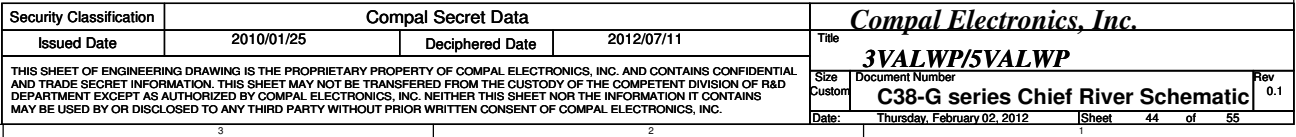
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Issued Date	2010/01/25	Deciphered Date	2012/07/11	Title	PWR DCIN
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				Date:	Thursday, February 02, 2012
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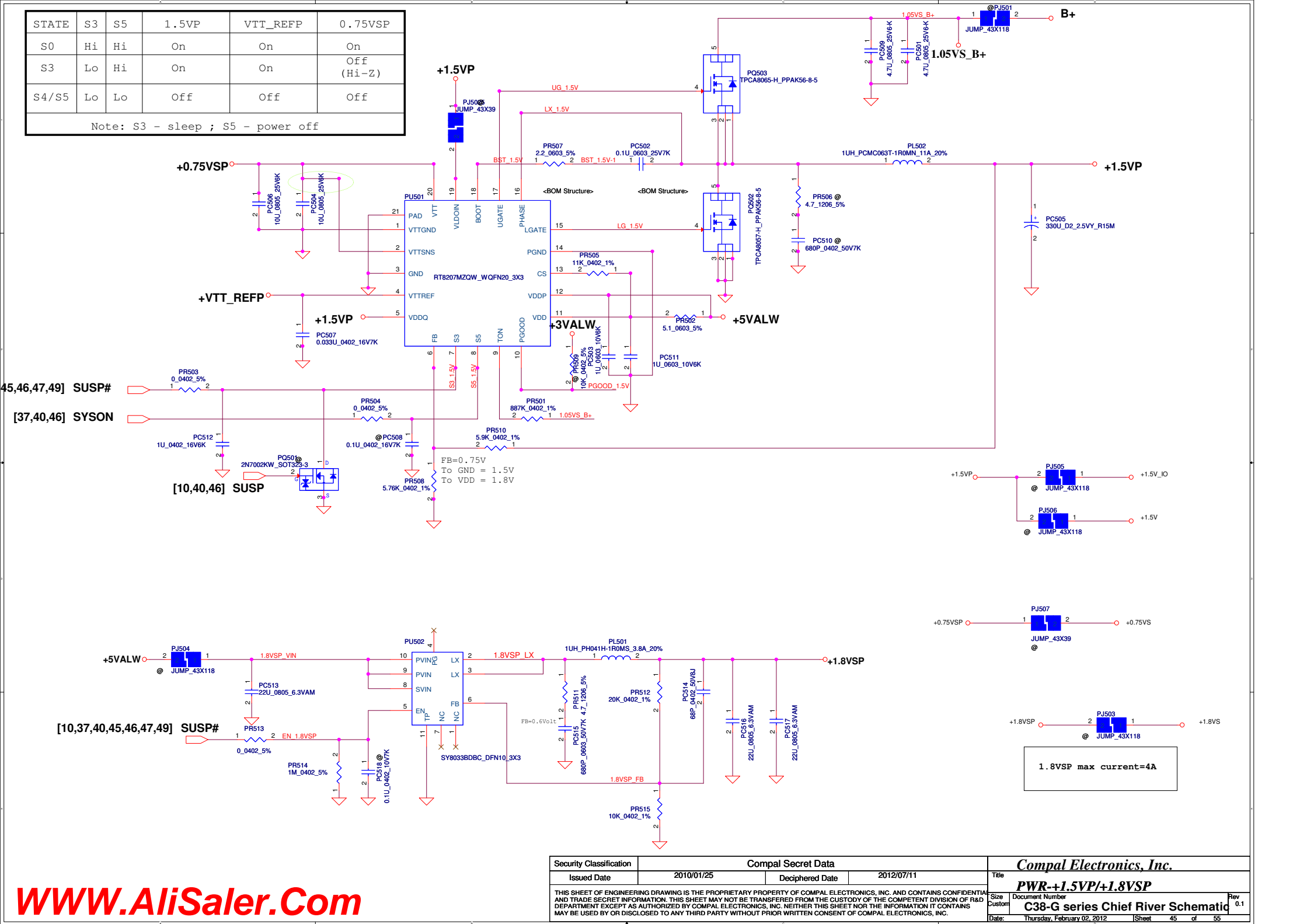




**WWW.AliSaler.Com**

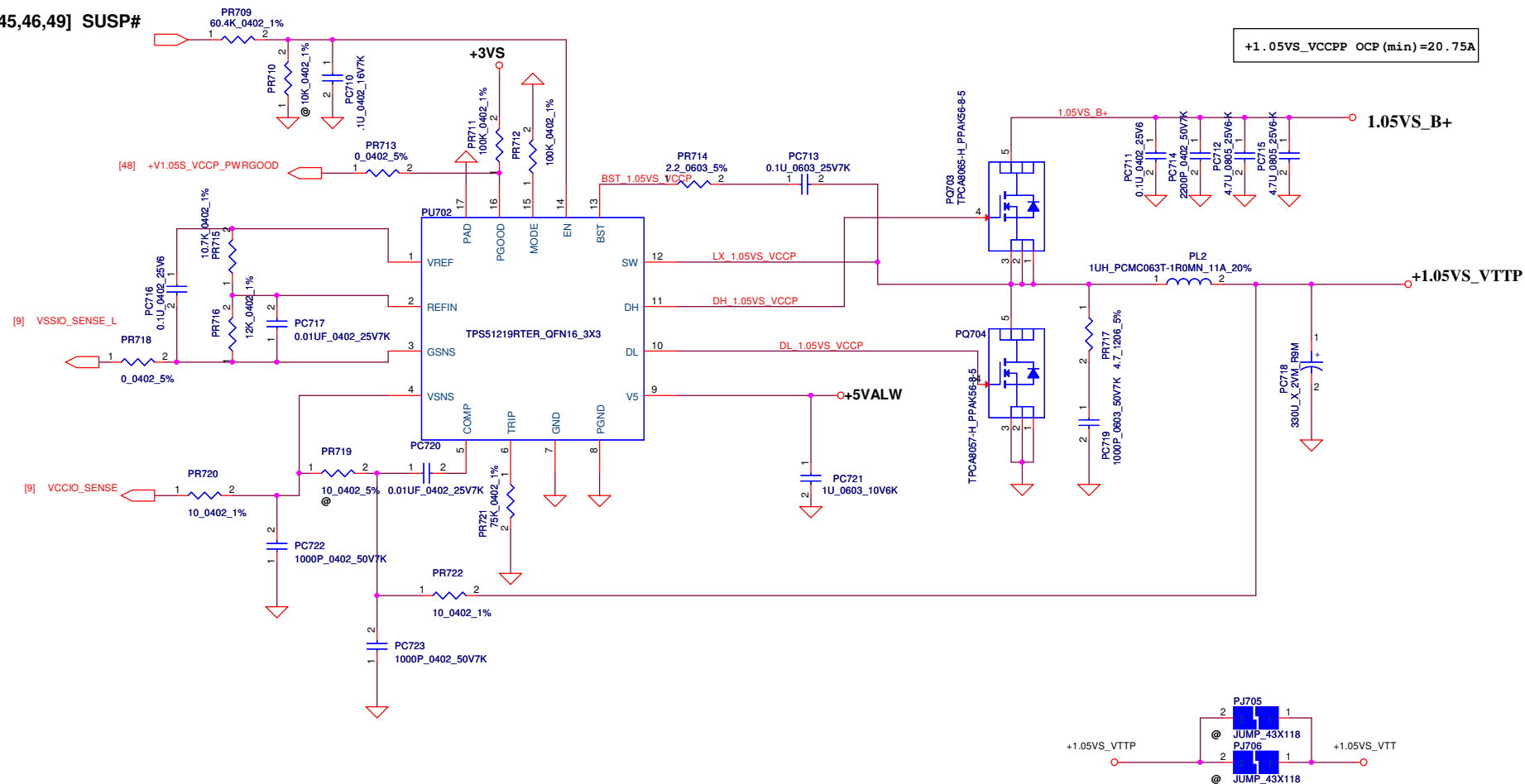


STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off
Note: S3 - sleep ; S5 - power off					





[10,37,40,45,46,49] SUSP#

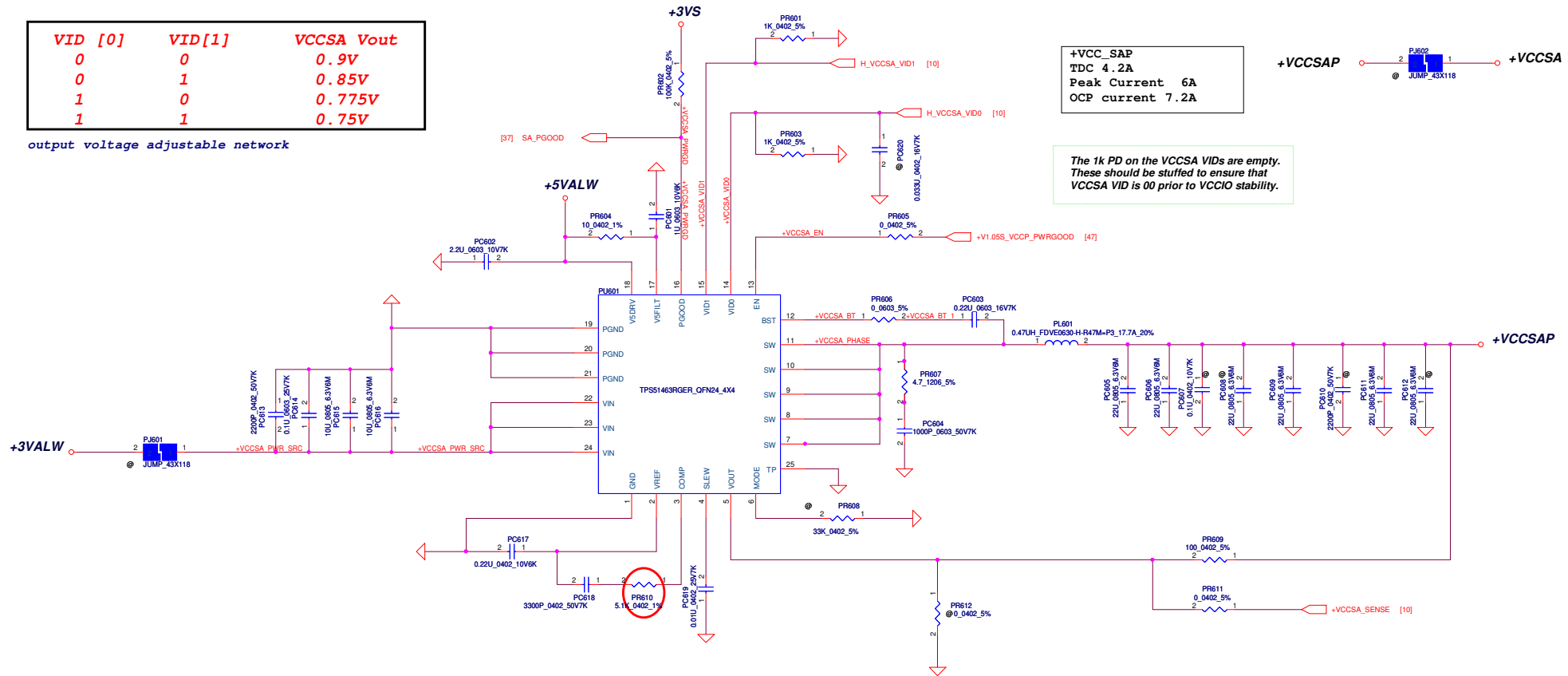


+1.05VS\_VCCPP OCP (min)=20.75A

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VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

output voltage adjustable network



+VCC\_SAP  
TDC 4.2A  
Peak Current 6A  
OCP current 7.2A

+VCCSAP  
+VCCSA  
+VCCSA

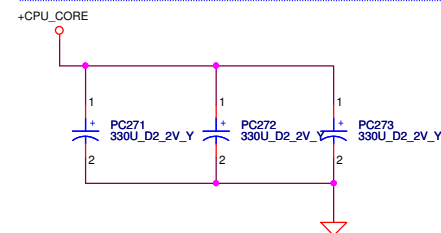
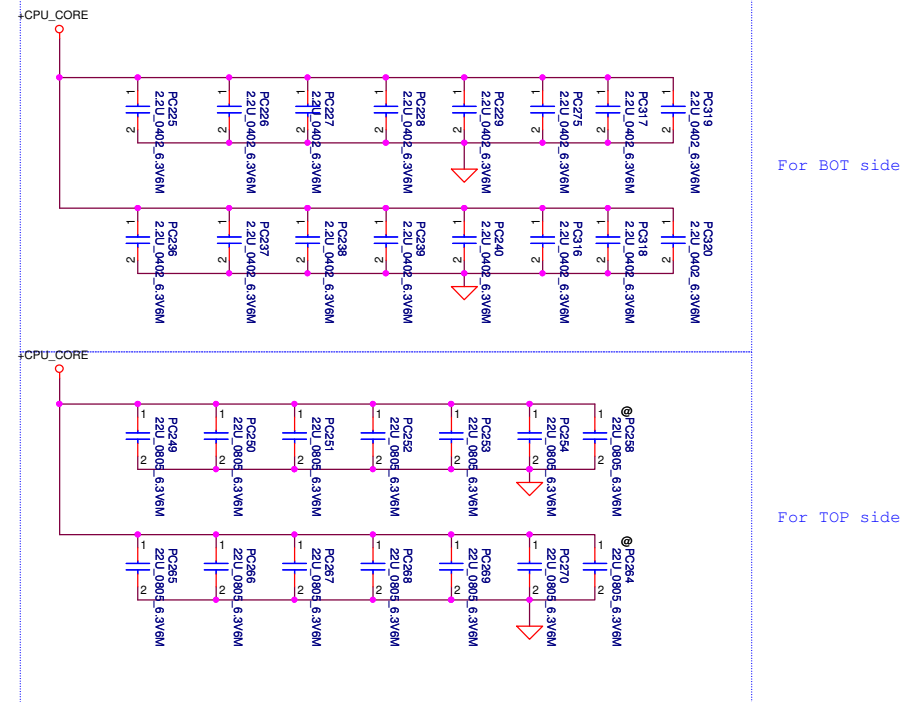
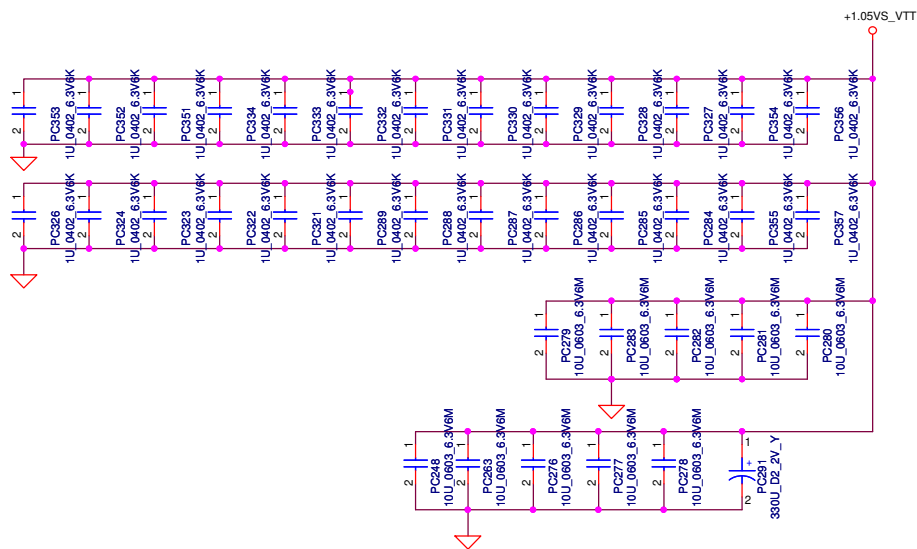
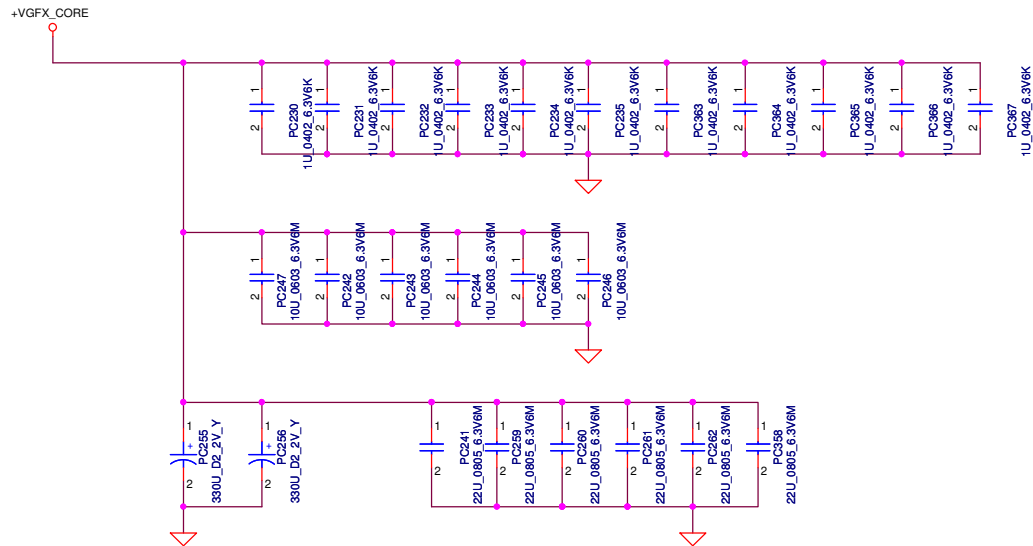
The 1k PD on the VCCSA VIDs are empty.  
These should be stuffed to ensure that  
VCCSA VID is 00 prior to VCCIO stability.

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								CPU_CORE_CAP	
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				C38-G series Chief River Schematic	
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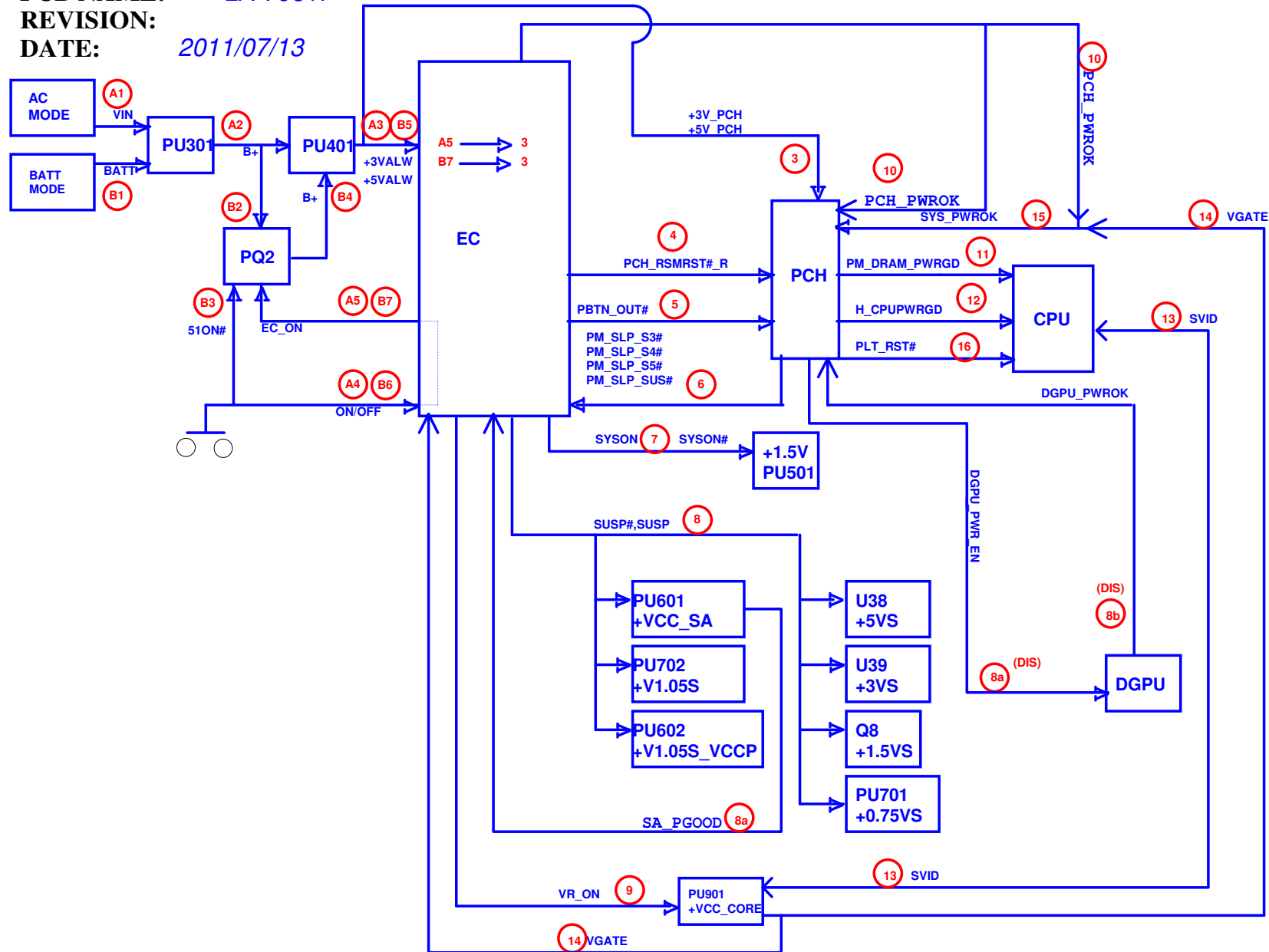
# COMPAL CONFIDENTIAL

MODEL NAME: *Power Sequence Block Diagram*

PCB NAME: *LA-7981P*

REVISION:

DATE: *2011/07/13*



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Item	Reason for change	PG#	Modify List	Date	Phase
1	Initial				DVT
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Date: Thursday, February 02, 2012				Sheet	54 of 55